A Robust PRML Read Channel with Digital Timing Recovery for Multi-Format Optical Disc

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Abstract—In this paper, a PRML read channel that supports multiple optical disc formats, *i.e.* CD, DVD and BD is presented. The read channel includes digital timing recovery that generates timing matched data by interpolation, which can acquire high controllability and stability with small hardware. PRML bit detection is applied to the read channel in order to reduce bit errors for severe channel condition such as BD and high speed DVD. Also, PR-level of PRML is adaptively controlled to compensate asymmetry and signal level shift due to defects. To support high operating speed, the read channel is designed in a 2x-parallel processing. The read channel uses a 115 MHz main clock, and can support up to 8x DVD, equivalent to a channel rate of 210 MHz.

I. INTRODUCTION

Since the compact disc (CD) was first developed in the 1970's, optical discs have been widely used as the storage media for AV and computer data. As multimedia and computer technology quickly advanced, new optical discs with higher density have become necessary. To meet such demands, the digital versatile disc (DVD) which can store up to 4.7 GB in the same dimension as the CD was developed in mid 1990's. Recently, the Blu-ray disc (BD) which can store up to 23 / 25 GB data in a single layer was developed for HD multimedia application. To store more data in the same dimension, the BD uses the laser with shorter wave length (405 nm), and has narrower track pitch (0.32 µm) than the DVD. Also, 17PP modulation code is used to increase the data density in the BD. To cope with higher storage capacity and channel rate, effective signal processing methods are required in front-end processors.

In this paper, a PRML read channel with digital timing recovery for CD, DVD and BD formats is presented. In conventional read channels for high-density optical discs, timing recovery with analog VCOs is normally used. In contrast, the read channel presented in this paper uses a full-digital timing recovery with interpolator. The advantage of this is that it is possible to acquire high controllability with low cost and without the problems that arise in analog circuits such as PVT variations and noise from other circuits.

II. READ CHANNEL STRUCTURE

The overall structure of the read channel is shown in Fig. 1. Laser emitted by the pick-up is reflected at the optical disc layer and collected by the pick-up unit. The reflected light is then converted to electrical signal and processed by the analog front-end circuit, which has filters and equalizers for filtering noise signal and boosting specific frequency signal. Analog signal from the analog front-end is digitized and sampled by the ADC with static clock. The signal from the ADC is digitally processed, and the bit data stored in optical disc are detected in the read channel.

The read channel is composed of two parts – digital timing recovery and partial response maximum likelihood (PRML) bit detector. The digital timing recovery generates frequency and phase matched data by using an interpolator and timing control block such as a frequency detector (FD) and a phase detector (PD). PRML bit detection is used for more probable bit detection.

III. DIGITAL TIMING RECOVERY

The timing recovery in this read channel is processed in digital by using interpolation scheme [1]. The interpolator generates timing matched data from sampled signals and feed-backed timing data. All blocks in the read channel use the fixed clock equal to the sampling clock used at the ADC, and the clock is not synchronized with the input signal. Therefore, the interpolator generates the timing matched data with flags, which mean valid data only if the flag is '1'.

A. Down/up sampling conversion & programmable filter

Sampling rate conversion is necessary to support various optical disc speeds of CD, DVD and BD. The signal from analog front-end is sampled with the fixed clock, and it is better to down-convert sampled signal for low speed discs.

Programmable FIR filter is used for filtering out high frequency noise. Its coefficients are selected to filter out non-signal frequency region for each optical disc operating speed.
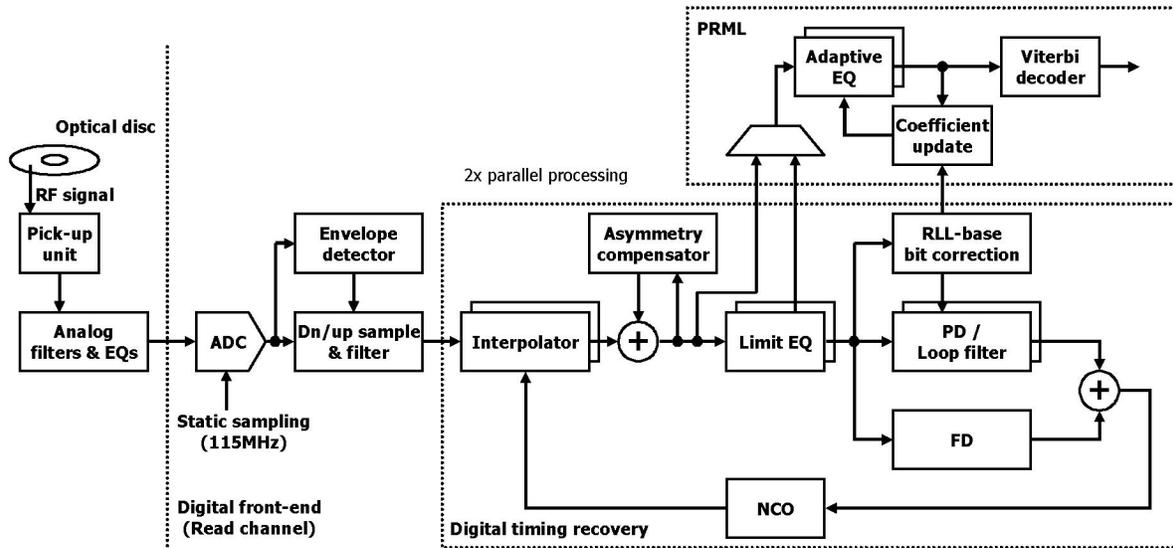
Figure 1.   Overall architecture of read channel

❖ Y[0] = μ[0]² x 0.5 x (X[3] - X[2] - X[1] + X[0]) + μ[0] x 0.5 x (-X[3] + 3X[2] - X[1] - X[0]) + X[1]
❖ Y[1] = μ[1]² x 0.5 x (X[4] - X[3] - X[2] + X[1]) + μ[1] x 0.5 x (-X[4] + 3X[3] - X[2] - X[1]) + X[2]
❖ μ[0] = Udto[0] / Idto[0], μ[1] = Udto[1] / Idto[1]
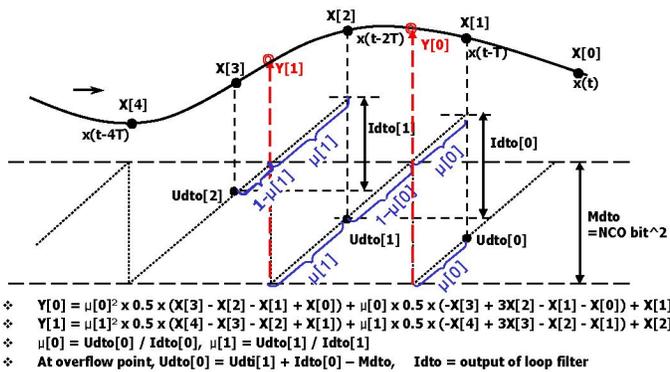❖ At overflow point, Udto[0] = Udti[1] + Idto[0] − Mdto,   Idto = output of loop filter

Figure 2.   Interpolator and NCO

The filtered signals are 2x up-sampled to support high speed operation. The ADC of this read channel samples the analog signal with 115 MHz clock, which is slower than the channel rate of the maximum operation speed of 210 MHz for 8x DVD. As bit data of optical discs are modulated that the minimum number of consecutive bits is at least 2, lower sampling than channel rate is sufficient for bit detection according to Nuquist theorem. The middle data of two sampled point is filled by up-sampling. It is possible to lower the sampling speed of an ADC by this method, but noise due to aliasing increases.

B.   Interpolator and NCO

The interpolator estimates the value at the phase-matched point of the input signal. Timing data generated by timing recovery loop are used for calculating the value of the phase-matched point. In this read channel, the interpolator uses 4 sampling data to calculate the value of the intermediate point as shown in Fig.2. To estimate the intermediate value precisely while reducing the hardware complexity, the interpolator adopts the parabolic interpolation method [2].

The numerically controlled oscillator (NCO) adds the output values of the loop filter every clock cycle. When the NCO value overflows, the interpolation flag is generated and intermediate ratio μ is calculated. For 2x parallel processing, the interpolator estimates the maximum 2 point values in one clock cycle as shown in Fig.2

C.   Asymmetry compensator & limit equalizer

The asymmetry compensator controls the baseline level which determines the '0' and '1'. Due to inadequate write power and various disc defects such as skew, eccentricity, vertical deviation and fingerprint, the baseline of the optical disc signal is fluctuated. The baseline is controlled so that detected bits are DC-free because recorded bit streams of optical disc are modulated to compress DC and low frequency components.

The limit equalizer is a non-linear equalizer specifically used for boosting high frequency signal of BD. It is described in detail in BD specification [3]. The middle value of two consecutive limit equalizer outputs is linearly interpolated and the sign of the middle value first determines whether the detected bit is '0' or '1'.

D.   RLL-based bit correction

The modulated NRZ streams of optical disc are RLL (n,k) codes, where n is the minimum consecutive number of '0' and k is the maximum number. Therefore, the minimum number of consecutive bit of the recorded signal should be n+1. The minimum run-length signals are easily disturbed by noise, ISI and asymmetry; hence detected bit streams can include RLL-violated bits. The RLL-based bit correction rule helps to correct miss-detected bits violating the minimum run-length. It uses the tendencies in the minimum run-length violation due to near-symbol interference. Fig.3 depicts an example of such rules for the BD. In Fig.3-(a), no RLL violation symbol exists, but the sign of the limit equalizer

output value is different from neighboring two detected bits. These two bits are corrected with inverting. In Fig.3-(b), there is a bit with run-length is 1, that violates minimum length. In that case, absolute values of near two limit equalizer outputs are compared, and smaller side bit is changed.

No RLL violation but sign of Limit EQ is different from neighboring two detected bits : change the two bit detections

Bit detection: ..., 1, 1, ...
Corrected: ..., 0, 0, ...   **(a)**

compare ABS value

RLL violation- run-length is 1 :compare absolute value of near Limit EQ output, and change the bit of smaller side

+ : Limit EQ output
O : The middle value of limit EQ outputs

Bit detection: ..., 1, 0, 1, ...
Corrected: ..., 0, 0, 1 ...   **(b)**

Figure 3.   RLL-based bit correction rule for BD
(a) Sign of limit EQ ouput is different from neighboring two detected bits
(b) RLL violated symbol detected

Zero crossing (bit corrected)

Timing error

baseline

+ : Limit EQ output
O : The middle value of limit EQ outputs

(a)

Timing error[1] → G3
Timing error[0] → G3

G1, G2 → Idto[1]
G1, G2 → Idto[0]

Z⁻¹

(b)

Figure 4.   (a) Timing function generation, (b) Loop filter

E.   FD, PD and loop filter

The FD tracks the channel rate frequency and helps the PD to quickly acquire locking. The FD first uses RLL violated data distribution to roughly track the frequency. Then, the FD compares the bit length of the detected frame with that of the correct frame and controls the NCO accumulation value until the difference comes within a certain range.

After the FD acquires the frequency lock, the PD starts tracking the input phase. Timing function for the PD is generated by similar method presented in [4], and controlled to be zero. When sign of two detected bits are different, that

is zero-crossing case; timing error is generated as shown in Fig.4-(a). The RLL-based corrected bit is used as detected bit.

The loop filter is a 1st IIR filter, and is designed to calculate the two timing function in one flag as shown in Fig.4-(b). Timing function gain G3 is controlled according to the PD state – tracking state and locking state. Controlling gain G3 is useful for fast locking and stable timing recovery operation.

IV.   PRML

The PRML is composed of an adaptive equalizer and a Viterbi decoder. The adaptive equalizer generates a defined partial response (PR) signal from the timing recovered data. The Viterbi decoder executes maximum likelihood sequence estimation (MLSE) from the output signal of the adaptive equalizer.

A.   Adaptive equalizer

The adaptive equalizer controls the tap coefficients by LMS algorithm applying power-of-2 method. Such method reduces hardware complexity by using shifter instead of multiplier and obtains more stable and fast saturation than the signed method. The adaptive equalizer uses RLL-based corrected bit streams for generating PR reference level as shown in Fig.5. The bits of the detected stream are multiplied each PR gain – a or b, and summed to generate current PR reference level. The difference of current reference value and the adaptive equalizer output is error value and used to updates coefficients of equalizer. This method can cause fault reference due to bit detection errors. However, bit errors concentrated on small run-length signals are partly corrected by RLL-based bit correction, so it is reliable to use detection bits for reference. This method is more stable than common blind adaptive equalization for signals distorted by defects on optical discs.

The adaptive equalizer can select output partial response in either PR (a,b,a) or PR (a,b,b,a) form. The PR (a, b, a) form is suitable for the output signal of limit equalizer for the BD, and the PR (a,b,b,a) form is suitable for signal bypassed limit equalizer. The adaptive equalizer processes two sampled data per one flag from digital timing recovery.

Reference[1]

Bit[0]

RLL-based Bit correction | Delay Control
Z⁻¹ Z⁻¹
Z⁻¹
Bit[1]

a 0 b a   b a
a 0 b a   b a

Reference[0]

ADEQ out[0]
ADEQ out[1]

Limit EQ | FIR filter (5-tap, 2x parallel)

Error[0]   Error[1]

Power-of-2 generation | Coefficients update

Figure 5.   Adaptive equalizer and coefficients update block

B. Adaptive Viterbi decoder

The Viterbi decoder also supports PR (a,b,a) and PR (a,b,b,a) form in a single structure. Fig.6-(a) shows the state transition diagram of Viterbi decoder for BD and CD/DVD, and Fig.6-(b) shows the modified transition diagram for processing 2 bits in one flag. It is sufficient to use only 4 states for BD because the minimum run-length is 2. However, 6 states are also used for BD to support CD, DVD and BD in a same structure.

The Viterbi decoder adaptively updates the reference transition levels of each transition to compensate shifted PR level due to asymmetry and any other defects. A last bit stream of most probable sequence is selected from survivor memory, and current transition reference level for the selected stream is compared with corresponding delayed output of the adaptive equalizer. The difference is then accumulated for selected transition. If the accumulated value exceeds the threshold level, corresponding transition reference level is updated. This Viterbi decoder structure is shown in Fig.6-(c).
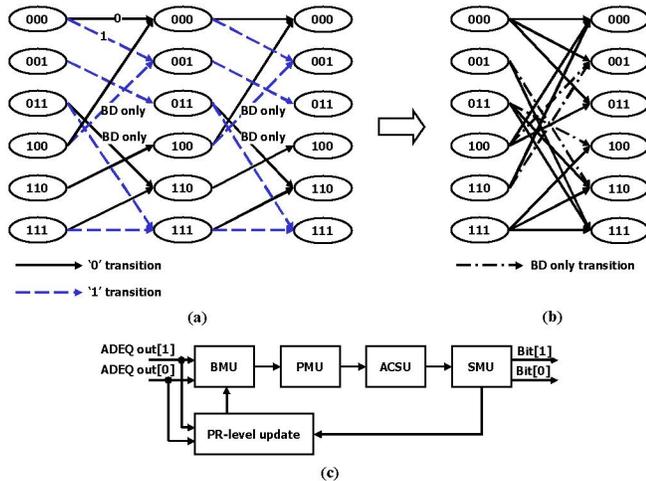
Figure 6. (a) 2 consecutive transition diagram,
(b) Modified transition diagram, (c) Adaptive Viterbi decoder architecture

V. SIMULATION RESULTS

Designed read channel is simulated using optical disc channel and asymmetry effect modeling introduced in [5]. In this paper, channel modeling applies 2x BD, and random Gaussian noise is added. Outputs of the modeling are sampled by an 8-bit ADC (ENOB = 7) with 115 MHz static clock.

Fig.7 shows the simulation result of SNR vs. BER. The PRML bit detection scheme shows significant improvement in bit error rate. Adaptive PRML method shows a little better performance than normal PRML. Fig.8 shows the simulation result of asymmetry vs. BER. Adaptive PRML method controls the reference transition levels to compensate shift by asymmetry, and also shows better performance than normal PRML.
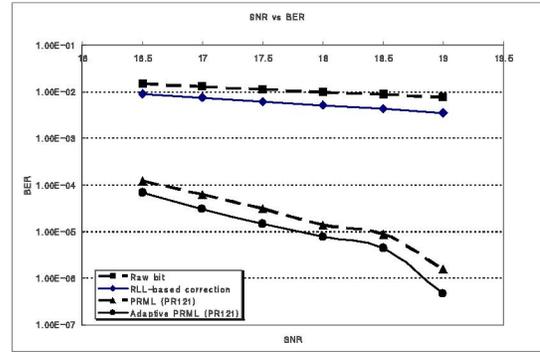

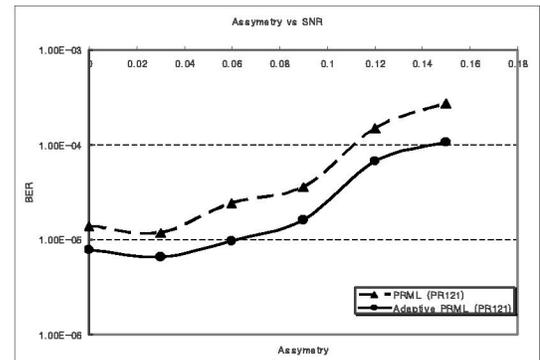Figure 7. Simulation result of SNR vs. BER

Figure 8. Simulation result of asymmetry vs. BER

VI. CONCLUSION

A read channel is designed to support CD, DVD and BD. The 8-bit ADC with 115 MHz clock is used for sampling analog signal from analog front-end. All digital bocks of read channel also use 115 MHz clock and designed in 2x parallel processing to support high speed optical disc – up to 8x DVD and 3x BD. The read channel is synthesized with TSMC 0.18 μm digital library, and gate counts is about 70k gates. That is approximately 0.70 mm², which is smaller than the read channels including analog VCOs for timing recovery. Adaptive PRML is applied for the read channel and shows better performance for noise and asymmetry.

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