DRAM Per- Row Activation Counting

양성필[§†], 강태운[§],   [§]

[§]고려대학교, [†]SK하이닉스

e- mail : yangs@ korea.ac.kr, taewoon_kang@ korea.ac.kr, gunjaekoo@ korea.ac.kr

Performance Analysis of a Per- Row Activation Counting Mechanism in DRAM

Seongpil Yang[§†], Taewoon Kang[§] and Gunjae Koo[§]

[§]Korea University, [†]SK Hynix

Abstract

In this study we evaluate the performance overhead of per- row activation counting (PRAC) mechanism employed in DDR5 DRAM. PRAC is designed to handle the security attacks against DRAM cells by enabling refresh to target and adjacent rows based on access counts since the last activation. However, PRAC requires additional peripheral circuits that increase DRAM timing and refresh counts, thus PRAC may provoke significant performance over- head.

 In order to investigate the performance hurdles by PRAC in DRAM, we analyze the performance impacts by adjusting DRAM timing parameters and refresh controls when PRAC is enabled in DRAM. We use the cycle- accurate DRAM simulator to evaluate the performance changes by various PRAC configurations. Our evaluation exhibits the per- formance overhead by PRAC is 8.5% on average when PRAC configurations are set up based on the JEDEC DDR5 standard.

I.

AI

DRAM

.   DRAM

DRAM

.   DRAM

DRAM

.   DRAM

DRAM

.

DRAM

.

Row Hammer(RH)   DRAM

row   row

,

[6].

.   DRAM

(row)

row   row   Tar-

get Row Refresh(TRR), DRAM   (parity)

On- Die ECC,

RH   [9,10].

.

Refresh Management (RFM)   row   PRAC
,   row   RFM   ,

[1].   Denial- of- Service(DoS)
RFM   .

,   PRAC   row

.   ,   .

Per- Row Activation Counting
(PRAC)   DDR5   [1].   2.3 PRAC
PRAC   row   PRAC   DRAM
row   .
.   tRP, tRC, tRFM   PRAC
PRAC   ,   .
,   DRAM   , DRAM

[5].   (tREFI)   PRAC
. tREFI

II.

. tREFI
2.1 PRAC   row   , RH
PRAC   DRAM   row   PRAC
row   .   .
PRAC   DRAM   RH   (N_{RH})   PRAC
row   Activate(ACT), Refresh(REF), Refresh   ,
management(RFM), Multi Purpose Command(MPC   . N_{RH}
- Manual ECS)   ,   ,
DRAM   ALERT_n   .
.   RFM   PRAC
row   row   .
[1,4].   ,

RH   .
PRAC   Adaptive Threshold   3.1 Simulator   PRAC
,   DRAM
[1].   Ramulator 2.0   PRAC
[5]. Ramulator 2.0   (yaml)   1
2.2 PRAC   ,   2
PRAC   row   ,   DRAM   , PRAC
RH   .
,   PRAC   ,
. ,   row   Per- Bank   row
. ACT   row
row   ,   ALERT_n
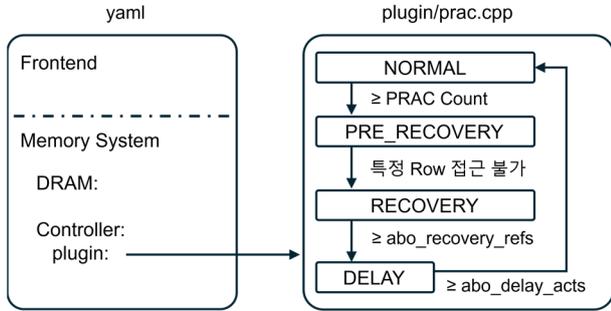tRP, tRC, tRFM   DRAM   PRE_RECOVERY
[1].   ,   RH

RFM   RECOVERY
. RECOVERY   NORMAL   .
abo_threshold, abo_delay_acts, abo_recovery_refs,
abo_act_ns   ,
N_{RH} .

1. Ramulator2.0 PRAC

3.2
                DRAM   PRAC
                              DRAM
Ramulator 2.0   [5].
                         1
         .   4.8GHz   ,
4- wide issue   128
4   1   . Last- Level Cache
64B cache line   8MB   .
               /
64   ,   FR- FCFS
        ,   RoBaRaCoCh   .
                DDR5- 3200   ,   1
2   .

1.

Processor	4.8GHz, 4 Cores/1 Core, 4- wide issue, 128- entry instr.
Last- Level Cache	64- byte cache line, 8MB
Memory Controller	64- entry read/write request queues; Scheduling policy: FRFCFS; Address mapping: RoBaRaCoCh
Main Memory (DRAM)	DDR5- 3200, 1 channel, 2 ranks

SPEC CPU2006/2017
        (H) 15   ,   (L)
26   .
        HHHH, HHHL, HHLL, HLLL, LLLL
    5   ,
                                              ,
    ,
                              [7].

3.3
                    Weighted Speedup(WS)
                                                     .
N_{RH} 1024   20
PRAC
         .   JEDEC
    ,   - 10%, 20%, 30%   .

        ,
                                            .
          PRAC
                              .
    WS   Ramulator 2.0
                          ,
        IPC   .   PRAC
off   WS   .
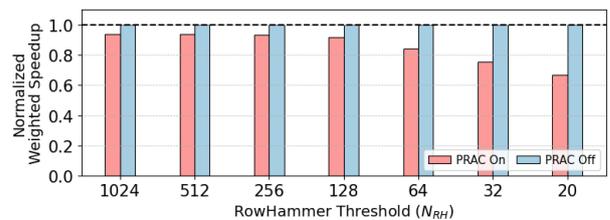
$$ WS = \sum_{i=0}^{3} \frac{IPC_i^{multi}}{IPC_i^{single}} \qquad Normalized\ WS = \frac{WS_{prac\ on}}{WS_{prac\ off}} $$

    , DDR5   LPDDR5   DRAM
    tREFI   , tREFI
        [1,2].

3.4
1) PRAC on/off
PRAC
                                        ,   PRAC on/off
        ,   .
        ,   2   , PRAC on
        N_{RH} 1024   256
6.2%   6.6%   ,
N_{RH} 128   8.5%
              . N_{RH} 128
                      , N_{RH} 20
    33.4%   .
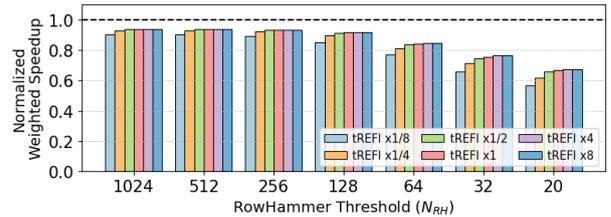 N_{RH} PRAC
                                  -
        .

2. PRAC on/off

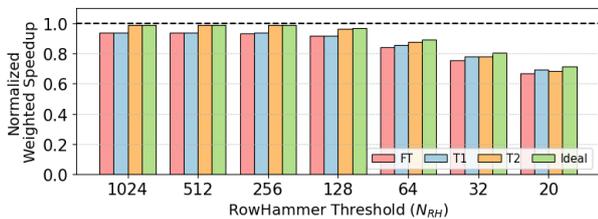   , JEDEC DDR5

                              30%

, N_{RH} 128   PRAC
.

2)
PRAC   row
      RFM   row   row
.
            ,   .

                        .
              (T1)
          (tRP, tRC)   ,   (T2)
row   row   tRFM1,
tRFMsb   .
              ,   T1   T2   Full
timing(FT),   T1   ,   T2
        ,   Ideal
        ,   3   FT   T1
N_{RH} 128
          ,   T1
                    .   , N_{RH} 128
                T2
        ,   RECOVERY
                    ,   RFM
          T2   .
  , Ideal
                    , N_{RH} 128
                .
        , PRAC   -   RFM
                                              -
          .

3.

3) tREFI
DDR5   JEDEC   32ms
8192   row   ,
          tREFI x1(3.9us)   .
    85' C   , tREFI x1/2(1.95us)
              [1].   ,
                    LPDDR5   tREFI x1/8

x8   , LPDDR6   PRAC
      [2,3].
          6   tREFI   (x1/8, x1/4, x1/2, x1,
x4, x8)   .
                        tREFI
                    ,   tREFI
  PRAC off   .
4   , N_{RH} 256
          PRAC on/off N_{RH}
                                .   ,
              tREFI
  , x1/2   6.7%
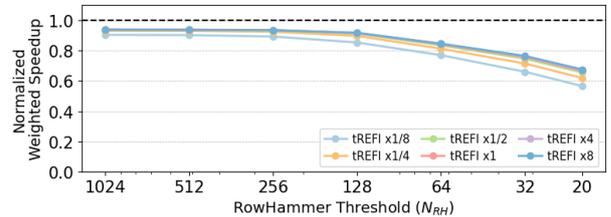   ,
              x1/4   x1/8
7.7%, 10.9%   .
                                        T1
      , tREFI
tRFC   ,   PRAC on   tRP
tRC
              .

4. tREFI

      ,   5   ,   tREFI
x1/4   x1/8
                            , tREFI

              .

5. tREFI

        PRAC
    N_{RH},   , tREFI
              .   , N_{RH} 128
      8.5%   PRAC
          , N_{RH} -

. , tRP, tRC

, RFM N$_{RH}$

. tREFI

tREFI ,

PRAC ,

. PRAC

, JEDEC

.

.

4.1

DDR5 DRAM RH

PRAC ,

. PRAC row

, ,

. , PRAC

, N$_{RH}$ 128

,

.

PRAC RH

,

PRAC

.

4.2

Ramulator 2.0

PRAC

,

cycle- accurate CPU

[8].

, ,

PRAC

.

,

RH DoS

PRAC

,

.

Acknowledgement

[1] JEDEC, DDR5 SDRAM, JESD79- 5C.01_v1.31

[2] JEDEC, LPDDR5 SDRAM, JESD209- 5A

[3] Murdock, Brett. LPDDR6: A Deep Dive Into the JEDEC Press Release. JEDEC Mobile / Client / AI Computing Forum, May 2024. JEDEC

[4] Bennett, Tanj, et al. "Panopticon: A complete in- dram rowhammer mitigation." Workshop on DRAM Security (DRAMSec). Vol. 22. 2021.

[5] Luo, Haocong, et al. "Ramulator 2.0: A modern, modular, and extensible dram simulator." IEEE Computer Architecture Letters 23.1 (2023): 112- 116.

[6] Kim, Yoongu, et al. "Flipping bits in memory without accessing them: An experimental study of DRAM disturbance errors." ACM SIGARCH Computer Architecture News 42.3 (2014): 361- 372.

[7] Canpolat, Oğuzhan, et al. "Understanding the security benefits and overheads of emerging industry solutions to dram read disturbance." arXiv preprint arXiv:2406.19094 (2024).

[8] Binkert, Nathan, et al. "The gem5 simulator." ACM SIGARCH computer architecture news 39.2 (2011): 1- 7.

[9] Bains, Kuljit, et al. Target Row Refresh Command for a Semiconductor Memory Device. U.S. Patent Application US20140059287A1, Intel Corporation, 27 Feb. 2014.

[10] Kang, Uksong, et al. "Co- architecting cont- rollers and DRAM to enhance DRAM process scaling." The memory forum. Vol. 14. 2014.