Can Systems Extend to Polymer? SoP Architecture Design and Challenges

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***Abstract*—Mechanically flexible and conformal shaped electronics is gaining momentum in today's electronics ecosystem. Rapid progress at device and circuit levels are already underway, but researchers are yet to envision the system design in a flexible form. This paper introduces hybrid flexible systems, and coins the term *System-on-Polymer (SoP)* to combine the advantages of flexible electronics and traditional silicon technology. First, we formally define flexibility as a new design metric in addition to existing power, performance, and area metrics. Then, we present a novel optimization approach to place rigid components on to a flexible substrate while minimizing the loss in flexibility. We show that intuitive placement leads to as much as 5.7x loss in flexibility compared to the optimal placement. Finally, we discuss major challenges in the architecture and design of SoPs.**

I. INTRODUCTION

Mechanically bendable, rollable, conformal, or elastic circuits, commonly known as flexible electronics, are emerging as a promising alternative to conventional rigid circuits. Flexible electronics are lighter, thinner and less expensive to manufacture [17]. Hence, they can enable wearable systems, such as electronic shirts, ties, and fire-fighter jackets, as well as arbitrarily shaped objects like electronic labels. Current successful examples of flexible electronics include displays [4], sensors [21], photovoltaic cells [27], batteries [14], simple micro-controllers, and radio frequency (RF) transmitters [1]. Despite their huge potential in terms of new applications, flexible electronics suffer severely from lower degrees of integration, limited performance and larger parameter variations compared to the state-of-the-art silicon technology. For example, silicon technology offers 14 nm feature size with an operating frequency in the order of 2 GHz, while feature sizes of thin-film transistors (TFT) range from $8\ \mu\text{m}$ to $50\ \mu\text{m}$ [10], and frequencies hardly exceed a few MHz [13].

While the huge capacity gap can be reduced by novel approaches such as carbon-based semiconductors [24], flexible electronics are far from implementing a full-fledged multiprocessor system-on-chip (MpSoC) with power and performance figures competitive with silicon technology. Current flexible electronics technologies include, inorganic and organic TFTs [26], as well as thin layered CMOS [1]. In analogy to early days of silicon CMOS, these efforts are extremely important, but focus on device, transistors and simple circuits. Given that leading manufacturers have started demonstrating flexible displays, complete system design on flexible substrates is a timely problem. Since using the flexible transistor technology alone does not provide competitive performance with existing MpSoCs, we propose *hybrid flexible electronics* for implementing complete systems on flexible substrates. The term *hybrid* implies integration of flexible substrates and circuits with rigid ICs. Since the most common flexible substrates are plastic, polymer and paper, we coin the term SoP, which stands for *Systems-on-*{*Polymer, Plastic or Paper*}. The idea behind this hybrid approach is to use silicon ICs where high performance, processing and storage capabilities are needed, while reverting to flexible electronics for everything else to maintain the benefits of flexibility.

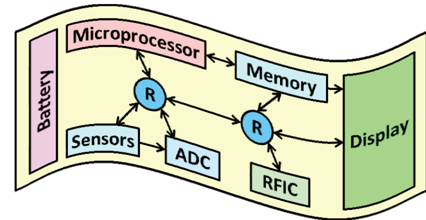

Fig. 1: An SoP with battery, sensors, ADC, microprocessor, memory, RFIC and display connected by flexible routers.

Our overarching goal is to implement a complete system architecture such as the one illustrated in Figure 1. By integrating flexible display, sensors, and battery with conventional chips, this generic architecture allows for a wide spectrum of systems ranging from simple internet-of-things (IoT) devices to complete mobile platforms like smart-phones. Systems-on-polymer have the potential to transform personal computing by enabling arbitrary shaped wearable systems not limited to desks, laps or hands. Towards achieving this goal, we introduce the SoP architecture, and investigate the use of SoPs for truly wearable computing systems. In particular, we propose *flexibility* as a new design metric in addition to the standard performance and area metrics. We demonstrate that flexibility is not only an important metric on its own, but it also results in interesting tradeoffs with performance and area. Introducing flexibility inevitably introduces novel challenges such as placement of rigid ICs onto flexible substrates, and aggravates existing communication, reliability, power and thermal challenges. As a result, there is a need for new design tools and methodologies that consider flexibility as one of the primary metrics. The major contributions of this paper are as follows:

- Defining flexibility as a new design metric in addition to area, power, and performance,
- Introducing SoP architectures and discuss corresponding design challenges,
- A methodology for the optimal placement of rigid ICs on a flexible substrate to minimize the loss in flexibility.

The rest of this paper is organized as follows. Section II contains the related research. Section III presents the analysis and optimization framework for flexibility as a new design metric. Section IV discusses the architectural challenges and new design problems. Section V concludes the paper.

II. Related Research

Several institutions have recently demonstrated the feasibility of flexible electronics [1, 4, 8]. For example, flexible 8-bit MCU, ADC, and RFIC have been successfully manufactured using TowerJazz CS18 PD-SOI CMOS process. This hybrid approach to manufacturing flexible electronics uses lower CMOS technology nodes, then converts the circuit to flexible form-factor [1]. Fully flexible asynchronous MCU and SRAM have also been developed using low-temperature poly-silicon TFT technology [7]. Finally, integrated programmable logic circuits have been recently demonstrated in [22]. We refer the reader to [12] for a comprehensive overview of flexible electronics and associated design automation challenges.

Since flexible components have significantly lower performance compared to CMOS technology, using hybrid flexible electronics is encouraged by national research agencies [23]. However, only a handful of studies addressed the design of hybrid system design to date. Hu et al. [9] have recently presented a hybrid self-power system that combines sensing capabilities and long-range interconnects of large area flexible electronics with the processing advantages of CMOS ICs. In [16], the authors present interface circuits between flexible electronics and CMOS ICs using capacitively-coupled signals. This paper takes a system level view and considers optimal integration of many macro-resources such as processor, display and sensors. We optimize the placement of the rigid ICs by modeling flexibility explicitly, and discuss the design challenges of SoP architectures.

III. Optimum Placement of Rigid Components on Flexible Substrates

Physical flexibility is a new design dimension that has not been considered by computer system designers so far. In order to incorporate flexibility in the design process, we quantify the maximum deflection of a flexible substrate as a measure of flexibility. This formalism enables us to treat flexibility as a *measurable* design metric. For example, it becomes possible to minimize the loss of flexibility under power/performance constraints, or impose a constraint on the loss in flexibility due to a rigid component. Then, we develop a design methodology for *optimally* placing rigid components on a flexible substrate with the objective of minimizing the loss in flexibility.

Consider a simple hybrid flexible system with one rigid component placed over a flexible substrate, as illustrated in Figure 2. We assume that the flexible substrate is a flat, homogenous isotropic material with uniform thickness. Figure 2 shows four pairs of uniformly distributed major bending forces that can be applied on the flexible substrate. All forces are normal to the plane of the flexible surface and uniformly distributed along the bending axis. We use the maximum deflection on either side to examine flexibility loss, as described next.

A. Flexibility Loss in Hybrid Flexible Systems

To analyze the impact of the relative size of a rigid component on flexibility, we consider a rigid IC of dimension $2l \times 2l$ mounted over flexible substrate of dimension $2L \times 2L$, as shown in Figure 2. We model this hybrid flexible system using two cantilever beams. First, the side-view of the flexible substrate alone and equivalent forces with pivot point are

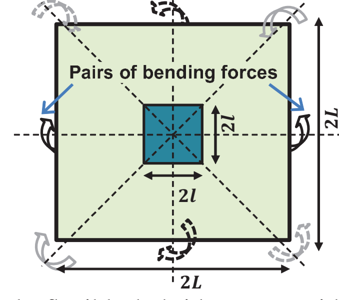

Fig. 2: A simple flexible hybrid system with one rigid component mounted over a large flexible substrate. Four possible uniform bending-force pairs are shown.

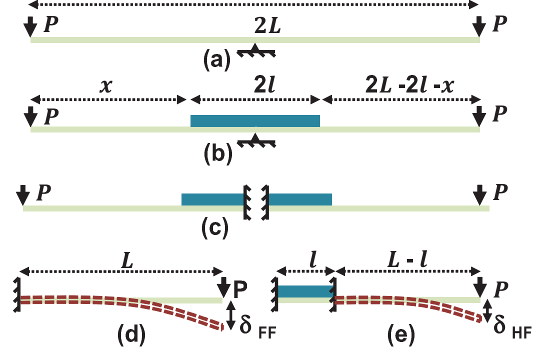

Fig. 3: Procedure for modelling the hybrid flexible system as a cantilever beam problem with special case, $x = L - l$.

shown in Figure 3(a). Then, the corresponding view for the hybrid flexible system is repeated in Figure 3(b). We analyze the deflection at the sides as two separate cantilever beams, as shown in Figure 3(c). In reality, the shear stress at the pivot will make some difference in the analysis of the pivoted beam and cantilever, but it is marginal and can be neglected due to thin flexible substrate. Cantilever beams with and without the rigid component are shown in Figures 3(d) and 3(e), respectively. Figure 3(e) shows that adding a rigid component decreases the effective length of the cantilever beam.

We can express the maximum deflection in a cantilever beam as a function of the uniformly distributed force P applied at one end (point force), modulus of elasticity E, and moment of area I [3]: $\delta_{\max} = \frac{L^3.P}{3.E.I}$. Hence, the maximum deflection in the fully flexible (δ_{FF}), and hybrid flexible (δ_{HF}) systems shown in figures 3(d) and 3(e) are given by:

$$\delta_{FF} = \frac{L^3.P_{\max}}{3.E.I} \quad \text{and} \quad \delta_{HF} = \frac{(L-l)^3.P_{\max}}{3.E.I} \tag{1}$$

where $P_{\max}$ is the maximum force the substrate can sustain before breaking. If the contact (e.g., soldering) between the rigid component and flexible substrate is weaker than the flexible substrate, $P_{\max}$ will become smaller than actual material breaking force. Then, we can find the reduction in deflection using Equation 1 as:

$$\text{Deflection Loss} = \frac{\delta_{FF} - \delta_{HF}}{\delta_{FF}} = \frac{L^3 - (L-l)^3}{L^3} \tag{2}$$

Flexibility loss: The loss in flexibility is plotted in Figure 4 using Equation 2 as a function of the ratio between the lengths of rigid component and the flexible substrate. When

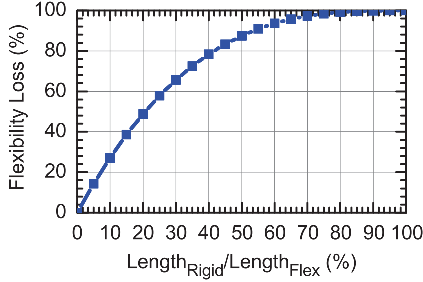

Fig. 4: The deflection flexibility loss in hybrid flexible system compared to fully flexible system with one chip.

the rigid component is 20% in length compared to the flexible portion, the deflection flexibility loss is 45%. We observe that increasing the area of the rigid IC quickly diminishes the flexibility. Since moving more functionality to the rigid ICs implies higher performance and area, Equation 1 enables analyzing the tradeoff between the new flexibility metric and classical metrics such as area and performance.

We have considered so far the scenario where the rigid IC is placed at the center for illustration purposes. If the rigid IC is placed at an arbitrary location x from one end point, as depicted in Figure 3(b), then the total displacement at both ends can be found as:

$$\delta_{HF} = \frac{x^3.P_{\max}}{3.E.I} + \frac{(2L-2l-x)^3.P_{\max}}{3.E.I} \tag{3}$$

B. Optimal Placement of Rigid Components

Next, we present a methodology to find the optimum placement of rigid components on a flexible substrate to minimize the flexibility loss. Longer distance between different rigid ICs imply longer interconnect on the flexible substrate, hence lower performance. Therefore, we first pack the rigid ICs into the smallest bounding-box with sufficient area left for interconnects using existing floorplanning techniques [2]. Then, we define this bounding-box as the rigid area, and find its optimal placement as a function of its dimensions, orientation, position and the bending axis.

Problem Formulation: The geometric representation of a generic problem instance is shown in Figure 5. Consider a flexible substrate $ABCD$, with the coordinates $A(0,0)$, $B(L,0)$, $C(L,L)$ and $D(0,L)$, respectively. The bounding-box $pqrs$ is placed with an arbitrary orientation angle θ with respect to the horizontal edge of flexible substrate. The area of the bounding-box B_A is fixed, while the length l and width b are free variables where $B_A = l \times b$. Let the coordinates of point r be (x_r, y_r), then the coordinates for points s, p and q can be expressed as:

$$(x_s, y_s) \equiv (x_r + b.cos\theta, y_r + b.sin\theta), \tag{4}$$
$$(x_p, y_p) \equiv (x_r + d.cos(\theta+\phi), y_r + d.sin(\theta+\phi)), \tag{5}$$
$$(x_q, y_q) \equiv (x_r + l.cos(\theta+\pi/2), y_r + l.sin(\theta+\pi/2)), \tag{6}$$

where $\phi = tan^{-1}(l/b)$ and $d = \sqrt{l^2+b^2}$.

The flexible substrate can be bent across an arbitrary bending axis such as a_1 and a_2 shown in Figure 5. For example, when the bending angle β (the angle between a_2 and x-axis)

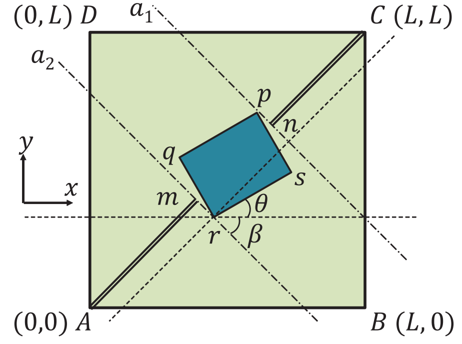

Fig. 5: Geometric illustration of an arbitrary bounding-box $pqrs$ with orientation θ over a flexible substrate $ABCD$ is shown. The bending axes a_1 and a_2 are parallel and equivalent to any other bending axis at an angle β and not intersecting the bounding-box region. $|\text{Am}|$ and $|\text{Cn}|$ are the lengths of cantilever beams.

is zero, the substrate is bent horizontally, i.e., along the x-axis. Likewise, $\beta = \pi/2$ implies vertical bending along the y-axis. We consider uniform bending all throughout the flexible substrate, and model the system using cantilever beams. Since deflection is proportional to the cube of length (Equation 3), the longest cantilever beam will give the largest deflection for a given amount of force applied. For example, consider the two cantilever beam models, $|\text{Am}|$ and $|\text{Cn}|$ shown in Figure 5. These cantilever beams are perpendicular to the two axes a_1 and a_2 and represent the largest length out of all other possible cantilevers. $|\text{Am}|$ and $|\text{Cn}|$ can be found as:

$$|\text{Am}| = x_r.sin\beta + y_r.cos\beta \tag{7}$$
$$|\text{Cn}| = (L - x_r - d.sin(\theta+\phi)).sin\beta + (L - y_r - d.cos(\theta+\phi)).cos\beta \tag{8}$$

In general, the total maximum deflection can be written as sum of deflections of these two cantilever beams as follows:

$$\delta(x_r, y_r, \theta, \beta, l, b) = \frac{P}{3.E.I}.[(x_r.sin\beta + y_r.cos)^3 + ((L-x_r-d.sin(\theta+\phi)).sin\beta + (L-y_r-d.cos(\theta+\phi)).cos\beta)^3] \tag{9}$$

Equation 9 gives the deflection for an arbitrary bending axis with angle β. Therefore, we can find the optimum dimensions l and b, orientation θ, and location (x_r, y_r) for the rigid bounding-box as a function of β. Depending on the usage scenario, we may want to bend the flexible substrate along multiple axes. For example, one might co-optimize for both horizontal and vertical bending instead of considering only one of them. Therefore, we define a set of bending angles, $\boldsymbol{\beta} = [\beta_1, \beta_2, \beta_3..., \beta_n]$ with respective relative importance $\boldsymbol{W} = [w_1, w_2, w_3, ...w_n]$. As a result, we can define the objective function as a weighted sum of deflections at different bending angles, and call it as the *maximum deflection*:

$$\Delta(x_r, y_r, \theta, l, b, \boldsymbol{\beta}, \boldsymbol{W}) = \sum_{i=1}^{N} w_i \times \delta_i(x_r, y_r, \theta, \beta_i, l, b) \tag{10}$$

Our goal is to maximize the deflection—the flexibility metric—under the geometric constraints. This can be expressed using a nonlinear optimization problem as follows:

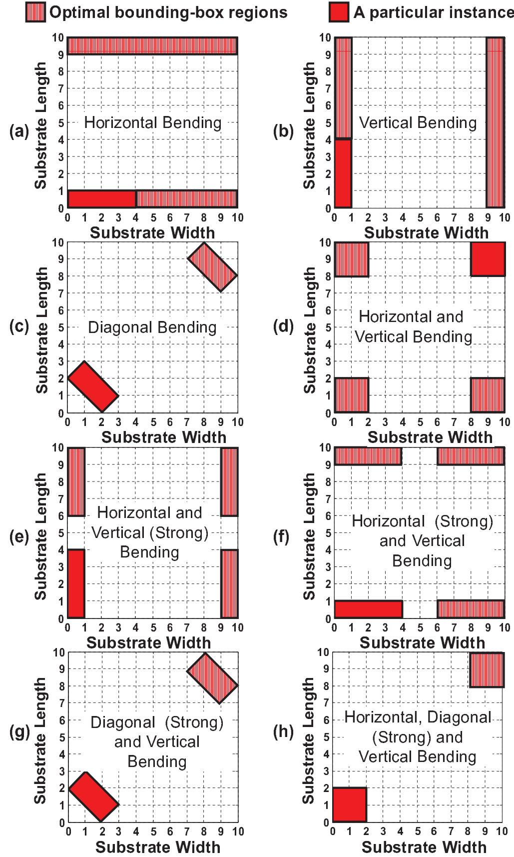

Fig. 6: Optimal bounding-box regions for the hybrid flexible system.

$$\begin{aligned}
\text{maximize}\quad & \Delta(x_r, y_r, \theta, l, b, \boldsymbol{\beta}, \boldsymbol{W}) \\
\text{subject to}\quad & g_c : 0 \leq x_r, y_r, x_s, y_s, x_p, y_p, x_q, y_q \leq L, \\
& g_\beta : 0 \leq \boldsymbol{\beta} \leq \boldsymbol{\pi/2}, \\
& g_\theta : -\min(\boldsymbol{\beta}) \leq \theta \leq -\max(\boldsymbol{\beta}) + \pi/2, \\
& g_l : l \geq L_{\min},\ g_b : b \geq L_{\min} \\
& \text{Area of bounding-box} : B_A = l \times b =, \\
& \sum_{i=1}^{N} w_i = 1,\ w_i \geq 0\ \forall i
\end{aligned} \tag{11}$$

The first inequality ensures that the bounding-box $pqrs$ remains within the flexible substrate boundary, while the second one constrains the bending angle g_β to the interval $[0, \pi/2]$. Similarly, g_θ constrains θ w.r.t. the maximum and minimum β values. The constraints g_β and g_θ avoid symmetric solutions. We also have constraints for the area B_A, minimum length g_l, and minimum width g_b of the bounding-box. Finally, weight of all bending angles sum to one, and all quantities except θ remain positive throughout the optimization.

C. Optimization Results

We solved the general optimization problem given by Equation 11 using numerical techniques in Matlab for 10 units $\times$ 10 units flexible substrate and a bounding-box with area $B_A = 4$ units^2. We also derived the analytical solution for special cases $\beta = 0$ and $\beta = \pi/2$ for validation purposes. Since the most common bending angles are horizontal, vertical and along the diagonal, we set $\boldsymbol{\beta} = [0, \pi/4, \pi/2]$ to analyze the optimal placements.

Figure 6(a) shows the optimal placement under horizontal bending ($\boldsymbol{W} = [1, 0, 0]$). The optimal orientation is $\theta = 0$, while the dimension of bounding-box is 4×1. This implies that the height of the optimal bounding-box comes out to be equal to the constraint, $L_{\min} = 1$. That is, the orientation is parallel to the bending axis and the dimension perpendicular to the bending axis is minimized as expected. Furthermore, we observe that the bounding-box can be placed at either side. This makes sense since the maximum displacement depends on the cube of the distance from the side, which is maximized when the bounding-box touches at either side. Similarly, for vertical bending ($\boldsymbol{W} = [0, 0, 1]$), the optimal orientation is $\theta = -\pi/2$, dimension of bounding-box is 4×1, and the placement is either at $x_r = 0$ or $x_r = 9$, as shown in Figure 6(b). When the bending is diagonal as in Figure 6(c), the orientation is $\theta = \pi/4$, as expected. We also note that the optimal dimensions are 1.41×2.83, which is non-trivial unlike the previous cases, while the placement was at either corner.

More complex scenarios with multiple bending angles are shown in Figures 6(d)–6(h). For vertical and horizontal bending together ($\boldsymbol{W} = [1, 0, 1]$), the output is $\theta = 0$, dimension of bounding-box is 2×2, and initial points are $(0, 0)$, $(0, 8)$, $(8, 0)$, and $(8, 8)$, as shown in Figure 6(d). Note that, the result is same irrespective of any amount of additional diagonal bending as shown in Figure 6(h). The results with $\boldsymbol{W} = [0.25, 0, 0.75]$ and $\boldsymbol{W} = [0.75, 0, 0.25]$, shown in Figures 6(e) and 6(f) are similar to Figures 6(b) and 6(a), but all regions are not included. For strong diagonal and vertical bending ($\boldsymbol{W} = [0, 0.75, 0.25]$), the result is similar to Figure 6(c), but has slightly different dimensions of bounding-box (1.46×2.73) and initial position $(0, 1.93)$. The tendency is to move the bounding-box towards the corners of the flexible substrate.

Intuitively, one might place the bounding-box at center with dimensions 2×2, similar to the placement in Figure 2. The comparison of maximum bending versus the result of this placement is shown in Table I. The optimal solution gives $4.58\times$ gain in flexibility on average. These results show substantial improvements in flexibility and signify the importance of optimal placement for wearable computing system design.

TABLE I: The gains in flexibility are shown by placing the bounding-box optimally (Δ^*) as opposed to intuitively placing it at the center (Δ_{center}) of the substrate with dimensions $10cm \times 10cm \times 300\mu m$, Elastic $E = 70.56GPa$ [25], and an applied force $P = 0.5N$.

Figure 6 index	Weight Vector			Max. Deflection (cm)		Gain in Flexibility
	W_0	$W_{\pi/4}$	$W_{\pi/2}$	Δ_{center}	Δ^*	
(a)	1.00	0.00	0.00	0.45	2.55	5.70 $\times$
(b)	0.00	0.00	1.00	0.45	2.55	5.70 $\times$
(c)	0.00	1.00	0.00	1.27	5.07	4.00 $\times$
(d)	0.50	0.00	0.50	0.45	1.79	4.00 $\times$
(e)	0.25	0.00	0.75	0.45	2.10	4.69 $\times$
(f)	0.75	0.00	0.25	0.45	2.10	4.69 $\times$
(g)	0.00	0.75	0.25	1.06	4.11	3.87 $\times$
(h)	0.20	0.60	0.20	0.94	3.76	4.00 $\times$

IV. SoP Architecture Design Challenges

In Section III, we proposed flexibility as a new design metric for wearable systems. Next, we overview major challenges in the design of SoP architectures, and analyze the interplay between flexibility and traditional design metrics.

A. SoP Communication Challenges

A flexible circuit can be bent into several millimeter radius before strain-induce damage to circuits. Bending the substrate can change the electron mobility by as much as 20%, and affect the timing of flexible circuits [20]. Moreover, physical changes in the substrate affect the interconnect capacitance, leading to further timing uncertainties. To analyze the effect of bending on flexible circuits, we implemented the ring oscillator given in Figure 7 using IGZO TFT technology [18]. SPICE simulations showed a nominal frequency of 175 kHz for this circuit. Then, we emulated the bending scenario described in Figure 8 by distributing the mobility variation according to the degree of bending, and analyzed the output frequency of the ring oscillator according to this mobility variation. Figure 8 clearly shows that the frequency follows the changes in bending. We also performed Monte Carlo simulations to validate our bending approximation by varying mobility in a Gaussian fashion. We found that the variation in frequency generated by the ring oscillator is between 150 kHz to 175 kHz, as shown in Figure 9. This frequency range is well within the bounds of frequency shown in Figure 8.

Since the bending axis and amount of bending cannot be known a priori, the changes in timing and clock period of printed circuits are unpredictable. Consider the circuit in Figure 10, which shows a combinational path between two registers. Bending can lead to setup and hold time violations as a function of the changes both in the delay of clock and combinational path. Designing for the worst case would deteriorate the performance, which is already suffering from low speeds and large feature sizes compared to silicon IC. What is more, techniques proposed to improve the reliability by dynamically detecting timing violations have also limited applicability since they would be also affected by bending. For example, we implemented the slack-probe technique [15] using TFTs to cope with timing variations. Our simulations showed that the circuit can hardly reach 500 Hz.

Timing and synchronization in flexible circuits are complicated by factors including supply-voltage, thermal, parameter variations, and bending. Therefore, asynchronous, or globally asynchronous locally synchronous (GALS) [19] communication, and latency insensitive design techniques [5, 6] are much better fit for SoP communication. GALS is particularly attractive since different synchronous rigid ICs can communicate over a network composed of asynchronous routers [19].

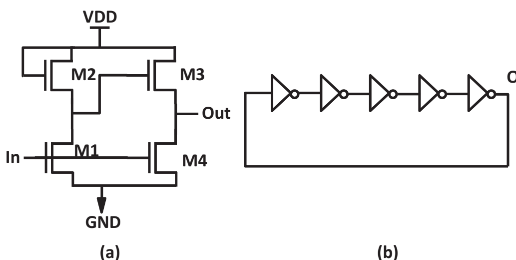

Fig. 7: (a) Design of basic pseudo-E CMOS inverter [11]. The W/L ratio used in this paper for M3 is $9\mu m/9\mu m$ and for all other transistors is $18\mu m/9\mu m$. (b) The circuit diagram of a ring oscillator made using pseudo-E inverters.

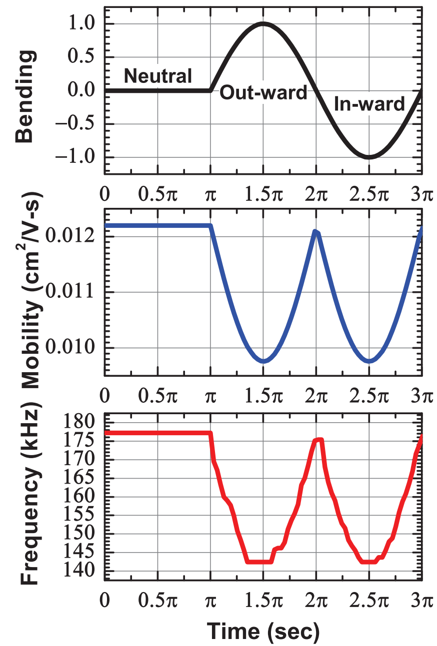

Fig. 8: The change in ring oscillator frequency because of change in mobility due to bending.

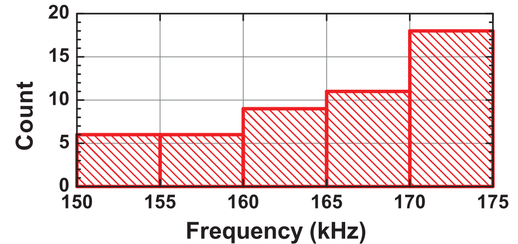

Fig. 9: Frequency histogram obtained by Monte Carlo simulation of the ring oscillator for 20% change in mobility.

B. SoP Design Challenges

Partitioning: While putting more functionality to a large conventional silicon IC would maximize the integration density, and deliver the largest processing capability, it could undermine the advantages of flexibility, and increase the manufacturing cost, power density, and surface temperature. The latter has utmost importance since these devices are expected to be worn and potentially touch users' skin. Furthermore, flexible electronics technology is changing rapidly to alter the cost/benefit dynamics [24]. Therefore, it is important to develop novel techniques for partitioning the functionality among multiple conventional ICs and flexible circuits while meeting the *quality objectives*, such as level of flexibility, surface temperature, power, and performance. This requires creating partitioning algorithms which have multi-level objective functions with tight quality objective constraints.

Power and Thermal Management: Future wearable systems, such as low-cost wristband that can be used in hospitals, baby monitoring systems and smart shirts for athletics, will be in contact with human body. Since neither active cooling nor traditional passive heat sinks can be used on flexible substrates, even a transient increase in power consumption, which could happen in the order of milliseconds, can rapidly raise the temperature. What is more, we need to cope with strain induced timing changes illustrated in Section IV-A using

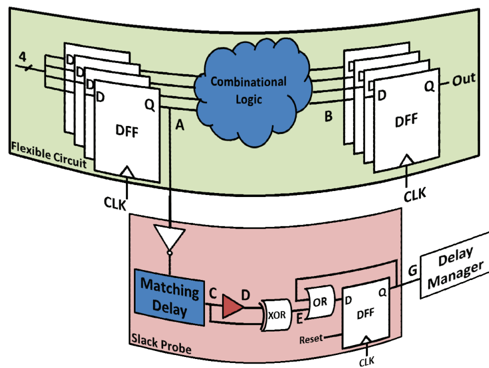

Fig. 10: Flexible circuit pipeline showing four input and four output registers with combinational logic. A slack-probe [15] has been inserted at point A, to detect delay failure.

dynamic voltage-frequency scaling. Therefore, novel cooling and thermal management techniques, as well as accurate power and thermal models targeting SoPs are needed.

Reliability: Different types of flexible transistors exhibit varying levels of reliability. In addition to the material properties, bending also affects the reliability, since it changes the electrical characteristics. For example, the drain current of the ultraflexible pentacene FETs changes by about 10% after 160,000 bending cycles [20]. As a direct result of material defects, flexible circuits—hence hybrid flexible systems—are prone to failures. The heterogeneity of the SoP architectures proposed in this paper can be used to provide fault-tolerance. Unlike traditional designs where area and wiring resources are scarce, the large area benefits of the flexible substrates can be used to provide redundancy in routers and network links.

Integration and I/O Interfaces: Integrating flexible substrate and rigid components together to form a hybrid flexible system poses unique interface and bonding challenges. There is a need for robust interfaces between the CMOS ICs and flexible circuit such as the one presented in [16]. The physical contact and adhesive (e.g., soldering) between the rigid component and flexible substrate determines the maximum breaking force $P_{\max}$ that can be applied to the get deflection, as discussed in Section III. A stronger bond will increase the flexibility of the material by allowing more force to be applied. Another challenge is getting data in and out of SoP architectures. Since traditional wired interfaces of USBs are not viable, SoPs will depend more on wireless interfaces using RFICs [1]. These interfaces should enable the wearable SoPs to seamlessly connect to the IoT devices with low power overhead.

V. Conclusion

This paper introduced the SoP architecture and discussed the use of SoPs for wearable computing systems. By combining the advantages of flexible electronics and silicon technology, SoP architectures offer a great potential in transforming wearable computing. However, there are many design and technology challenges in adapting SoP architectures. As the first step in addressing these challenges, we introduced the maximum deflection of a flexible substrate as a new metric in addition to traditional power, area and performance metrics. Using this new metric, we developed a methodology for the optimal placement of rigid ICs on flexible substrates to minimize the loss in flexibility.

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