Extending Networks from Chips to Flexible and Stretchable Electronics

Invited Paper

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***Abstract*—Emerging flexible hybrid electronics paradigm integrates traditional rigid integrated circuits and printed electronics on a flexible substrate. This hybrid approach aims to combine the physical benefits of flexible electronics with the computational advantages of the silicon technology. In this paper, we discuss the possibility to implement a physically flexible system capable of sensing, computation and communication. We argue that this capability can transform personalized computing by enabling the next big leap forward in the form factor design, similar to the shift from desktop and laptop computers to hand-held devices. Designing this type of a comprehensive system requires integrating many flexible and rigid resources on the same substrate. As a result, efficient interconnection network design rises as one of the major challenges similar to the system-on-chip experience. Therefore, we also discuss the interconnect design challenges and promising solutions for flexible hybrid systems.**

Keywords — Flexible Electronics, Flexible Hybrid Electronics, Systems-on-Chip, Thin-Film Transistor (TFT)

I. Introduction

Flexible electronics have the potential to transform computing by enabling bendable and stretchable systems with arbitrary shapes [39]. Physical flexibility combined with the cost and weight advantages opens a wide range of form factors and application areas, including wearable electronics, prosthetics, medical sensing, rollable displays, and internet of things (IoT) [32]. For instance, a brain-machine interface embedded on a hat or an electronic patch could enable controlling a prosthetic arm and interaction with IoT devices. However, performance and capabilities of purely flexible electronics are very limited [35]. Therefore, flexible hybrid electronics (FHE) has recently emerged as a promising technology to address these limitations [10]. FHE refers to physically flexible systems that integrate commercial off-the-shelf rigid integrated circuits (ICs) on flexible or stretchable substrates. Hence, the FHE concept combines the physical merits of flexible electronics with the power, performance and area advantages of traditional silicon technology.

During the last decade, tremendous advances in the system-on-chip (SoC) design enabled integration of a complete system including a large variety of processing elements and memory on a single die. This, in turn, gave rise to powerful yet low-power embedded platforms that enabled personal computing at a mobile form factor. We envision that the next big leap forward in form factor design can be enabled by flexible hybrid electronics. More precisely, FHE can be used to design arbitrary shaped, flexible or stretchable systems with integrated sensing, computing and communication capabilities, as illustrated in Figure 1. This capability can deliver the functionality of current smartphones and more in a truly pervasive form factor. We have recently coined the term system-on-polymer (SoP) to refer to this fully integrated solution [17]. An SoP implements the whole system similar to system-on-a-chip, but the flexible circuits and off-the-shelf rigid ICs are integrated on flexible or stretchable substrates using *FHE*.

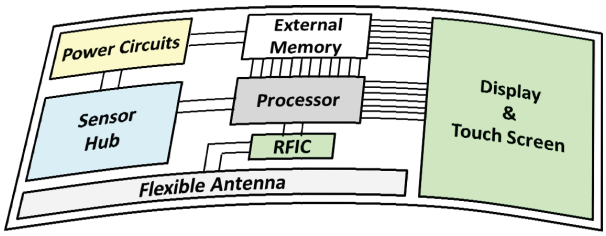

Fig. 1: An illustration of the future SoP, i.e., System-on-Polymer, concept.

Combination of sensing, computation and communication in a single system is possible only with the integration of many rigid ICs and flexible circuits. For example, the system illustrated in Figure 1 consists of a processor, off-chip memory, sensor hub, display, radio frequency IC (RFIC), printed antenna and voltage regulation circuitry. The SoC design experience shows that communication between these resources is critical for both the system performance and power consumption [27]. Therefore, the interconnection network should provide sufficient network and low latency such that communication does not become the performance bottleneck. Furthermore, battery constraints become even more stringent than SoCs due to the wearable form factor. This necessitates extreme energy-efficiency in all aspects of SoPs including the interconnection network design.

The communication challenge is amplified further by the evolutionary nature of flexible electronics. Most of the sensors, display and antenna are expected to be implemented using purely flexible electronics. With the current technology, the application processor, off-chip memory and RFIC will be

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likely rigid, since flexible electronics are not yet mature and competitive in these areas. At the same time, we witness great advances in the design of flexible processors, RFIC, analog to digital conversion and memory design [3, 14]. As the flexible electronics technology advances, the composition of flexible and rigid resources is expected to evolve. Consequently, the capabilities of SoPs are expected to flourish in time, while the interconnection networks adapt to the growing needs.

SoP interconnection network design challenge has two aspects. The first aspect is innovating reliable circuits and manufacturing solutions to interface rigid components with flexible substrates. This problem is addressed by novel interface circuits [23, 37] and recently funded manufacturing institute [29]. The focus of this paper is the second aspect, which is designing a system level communication network similar to networks-on-chip (NoCs) used in SoC and multicore chips [27]. We present system level communication challenges for SoPs, and discuss potential solutions to mitigate their effect. In particular, we analyze the system level interconnect solutions for two classes of systems. The first class of systems is bendable along an arbitrary axis, as illustrated in Figure 2(a). We refer to this type of systems as "*bendable*" throughout the paper. The second class is more comprehensive in the sense that they are "*stretchable*" as well as bendable, as illustrated in Figure 2(b). The communication bandwidth reduces dramatically from rigid to bendable, and bendable to stretchable systems due to lower integration density and lower operating frequencies. Furthermore, global interconnects on flexible substrates suffer from lower reliability, since they are prone to physical damage. As a result, wireless communication becomes advantageous both in terms of energy efficiency, performance and reliability. Therefore, we propose a hybrid combination of Low Voltage Differential Signaling (LVDS) [15] based communication and inter-chip wireless communication [6, 9].

The remainder of this paper is organized as follows. We overview the FHE technology and related literature in Section II. In Section III, we discuss the SoP interconnect design challenges and potential solutions. Section IV presents potential application areas of FHE. Finally, we conclude the paper by summarizing the key points in Section V.

II. Background and Related Work

Flexible electronics refers to integrated circuits implemented on bendable, stretchable, rollable, conformable, or elastic substrates which are lighter, thinner, and less expensive to manufacture [39]. Major building blocks of flexible electronics are the substrate, backplane electronics, frontplane and encapsulation. Common types of substrates are thin glass [26], plastic film [28] and metal foil [39]. Backplane electronics are used for processing and power/signal delivery to the frontplane. Most common materials used for backplane include silicon thin-film transistors (TFT) [25], organic thin-film transistors [41] and transparent thin-film transistors [24]. Interconnect and contacts are implemented using transparent conductive oxides, conducting organic polymers and stretchable wires. Finally, frontplane could be liquid crystal display, organic light-emitting display, an actuator such as an artificial muscle or sensor [25].

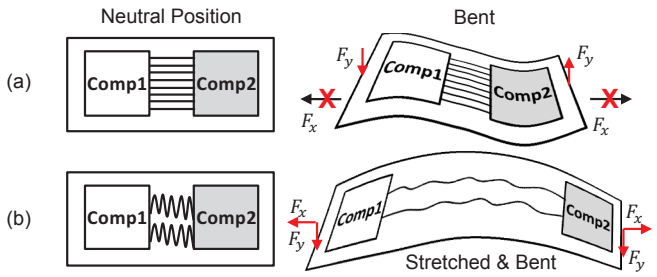

Fig. 2: The relaxed and deformed examples of bendable and stretchable SoPs. (a) The forces are only applied in y direction. (b) The forces can be applied in all three directions x, y, z. Figure shows forces in direction x and y only.

Flexible electronics technology has been used successfully to design displays, electronic paper, sensors, photovoltaic cells and batteries [33]. More recently, researchers have demonstrated wireless tags [20], programmable logic circuits [34], simple micro-controllers, analog-to-digital converters (ADC) and radio frequency transmitters [1]. However, performance and capabilities of flexible electronics is still significantly lower than that offered by CMOS technology [19]. Therefore, flexible hybrid electronics have been proposed to exploit the advantages of rigid ICs [29, 33]. Integration of CMOS devices on flexible substrates has been demonstrated recently [18, 35]. Moreover, circuits for interfacing flexible electronics and CMOS ICs have been proposed [23, 37].

Design of metal wire interconnects for stretchable electronics is presented in [16, 40]. The authors in [16] discuss three different shapes of metal interconnects on a polydimethylsiloxanes substrate using finite element analysis. Each interconnect is stretchable matrix of shape elliptical, U-shape and horseshoe. When deformation occurs, only the shape of the interconnect changes without any significant change in the resistance, because total length still remains the same. In addition to this, the work presented in [40] demonstrates a highly stretchable electronic system with free floating interconnect network. The network consists of serpentine shaped wires connecting assemblies like ICs that are suspended in a microfluid. Despite the impressive progress in the development and analysis of these interconnects, they have lower integration density and lower performance compared to on-chip interconnects. To mitigate these effects, approaches that use wireless communication for intra- and inter-chip communication can be used [6, 9], as detailed in Section III-B.

III. SoP Interconnect Challenges and Potential Solutions

A. Limitations of Wired Interconnects on Flexible Substrates

Bandwidth Limitations: The bandwidth of a communication channel can be expressed as $BW = W \times f_{max}$, where W is the number of links and f is the maximum frequency at which one bit can be transmitted over one link [22]. Compared to

SoCs, the communication bandwidth on flexible substrates is severely limited by three factors:

1) *Low integration density:* Modern CMOS technology and printed circuit board provide more than ten metal layers. Flexible and stretchable substrates, on the contrary, have limited number of layers putting larger constraints on the number of wires and wire pitch. Since a typical wire width is around 90μm [16], it can limit the wire pitch to $\sim$200μm for bendable and $\sim$800μm for stretchable systems. Moreover, the links on the substrate need to connect to the pins of the rigid ICs. Hence, even if smaller wire pitch becomes possible, still the physical dimensions of the rigid ICs impose limitations.
2) *Physical limitations:* Besides manufacturing challenges, adding more wiring layers is not desirable, since this decreases the flexibility of the system, as depicted in Figure 3. The flexibility reduces with more wires, since the elasticity of the interconnects is significantly smaller than that of the substrates. For example, the Copper wires have a higher Young's modulus of elasticity of 128GPa compared to Polyimide's elasticity of 7.5GPa [11].
3) *Limited circuit support:* Fast on-chip and on-board communication over long links (in the order of millimeters) is enabled by optimally inserted repeaters, designed using CMOS technology [7]. Since the TFTs are significantly slower, these techniques may not be a viable option for flexible interconnects.

As a result of low integration density (1) and physical limitations (2), the number of wires that can fit into a given cross-section (i.e. W) is a few orders of magnitude smaller for flexible electronics. Furthermore, the maximum signaling frequency f_{max} over long wires is limited due to limited circuit support (3). Consequently, the communication bandwidth on flexible substrates using conventional approach is significantly lower than that available for SoCs.

Shape Changes: The interconnect design challenge in flexible hybrid electronics is aggravated by the physical flexibility. Our measurements on an experimental prototype and finite element method (FEM) simulations show that bending does not change the length and electrical properties of Copper wires significantly. However, increasing the wiring area decreases the flexibility significantly, as depicted in Figure 3. In this figure, we show COMSOL simulation results for bending a Polyimide substrate. The abscissa equal to zero corresponds to a Polyimide substrate without any wires on it. We observe that the flexibility normalized to this point decreases significantly by adding Copper wires to the substrate. For example, if 30% of the total area is Copper interconnect, the maximum displacement of the substrate at the edge decreased by more than 22%, as illustrated on the plot.

The effect of the shape changes is more pronounced for stretchable substrates. As illustrated in Figure 2, a serpentine interconnect is used to accommodate length changes due to stretching [16]. This has two design drawbacks. First, the effective length of the wire is as long as the worst-case stretching, even when the substrate is in neutral position. Second, the serpentine shape further increases the area allocated for wiring reducing W, hence limits the available bandwidth.

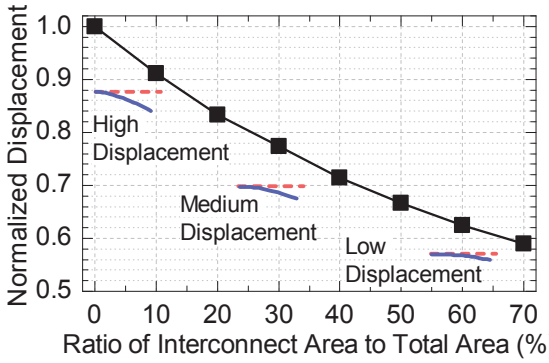

Fig. 3: Change in the deflection of the SoP with increasing interconnect area.

Reliability Limitation: Continuous physical deformation of the SoPs can decrease the reliability of flexible circuits and their interconnects as the number of bending cycles increases. For example, after 160,000 bending cycles of ultraflexible pentacene Field Effect Transistors, the drain current changes by about 10% [31]. This can cause some portions of the circuit to slow down and trigger timing violations leading to the failure of the device. Moreover, the contacts to the chip pins can break or get permanently deformed if too much stress is applied. Thus, it is important to improve reliability at both material and system level. For instance, structural duplication like redundant interconnects and graceful performance degradation methods can be used for improving the reliability [30].

B. Inter-Chip Communication over Flexible Substrates

Potential of short-range wireless transceivers for on-chip wireless communication has been demonstrated in [9, 42]. For example, the work presented in [9] shows that wireless communication is more energy efficient than wired communication for distances over 7mm. As described in Section III-A, the interconnects on flexible and stretchable substrates are more limited compared to on-chip interconnects. Therefore, using wireless communication is even more promising in the context of flexible hybrid electronics.

In the following, we present a high-level comparison of energy per bit between a LVDS interfaced channel and a wireless link. We perform this comparison as a function of the data rate to identify the operating regions in which each approach is more energy-efficient.

Wired communication energy: On-chip wires generally act as lossy RC transmission lines, while the off-chip wires behave as LC transmission lines due to larger wire lengths [8]. To drive these LC transmission lines, differential techniques like Low Voltage Differential Signaling, Emitter Coupled Logic, and Current Mode Logic are used. These differential

techniques, use a pair of electrical signals to transmit data, to minimize the effect of external electromagnetic interference. We choose LVDS, which is a low voltage, low power, differential signaling standard [15]. The power consumption of LVDS based interconnect consists of two components. The first component is the LVDS driver power consumption P_{driver}, while the second is the power consumption of the channel P_{channel}.

$$P_{\text{LVDS}} = P_{\text{driver}} + P_{\text{channel}} \tag{1}$$

The energy per bit can be obtained by dividing the power in Equation 1 by the data rate D_R,

$$E_{\text{wired}} = \frac{P_{\text{LVDS}}}{D_R} \tag{2}$$

For high frequency operations, long LC transmission lines cause channel attenuation, due to the skin effect and dielectric absorption [8]. We adapted a sophisticated channel model and parameters from [7] for a target bit error rate (BER) of 10^{-12}. Then, we computed the wire parameters assuming a Copper wire on a flexible substrate with the values summarized in Table I.

TABLE I: Parameter values for the 0.5oz Copper wires used in this paper.

Parameters	Values (mm)
Height	0.018
Length	100
Wire spacing	0.152

Wireless communication energy: The energy consumption for wireless transceiver depends on the power consumed in the transmitter and receiver circuits. We can express the power consumption for a wireless link $P_{\text{link,wireless}}$ as the sum of the transmitter power P_{Tx} and the receiver power P_{Rx}, i.e., $P_{\text{link,wireless}} = P_{\text{Tx}} + P_{\text{Rx}}$. The transmitter power can be further decomposed as the sum of the power consumption of the voltage-controlled oscillator P_{VCO}, frequency synthesizer P_{syn} and power amplifier P_{PA}.

$$P_{\text{Tx}} = P_{\text{VCO}} + P_{\text{syn}} + P_{PA} \tag{3}$$

$$= P_{\text{VCO}} + P_{\text{syn}} + \frac{1}{\eta}\gamma_{PA} L^2 D_R \tag{4}$$

where η is the PA efficiency, L is the transmission distance, and γ_{PA} is the path loss exponent [38]. Then, the energy consumed per bit can be found by dividing the total transceiver power by the data rate D_R as:

$$E_{\text{link,wireless}} = \frac{(P_{\text{VCO}} + P_{\text{syn}} + \frac{1}{\eta}\gamma_{PA} L^2 D_R)}{D_R} + \frac{P_{\text{Rx}}}{D_R}$$

$$= \frac{1}{\eta}\gamma_{PA} L^2 + \frac{(P_{\text{VCO}} + P_{\text{syn}} + P_{\text{Rx}})}{D_R} \tag{5}$$

We estimated the values in Equation 5 using an existing state-of-the-art on-off keying (OOK) CMOS transceiver design presented in [5].

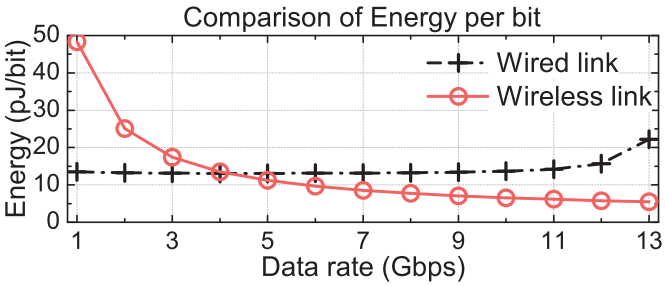

Fig. 4: Comparison of energy consumption per bit for wireless and wired links. The two curves intersect at 4.1Gbps.

Energy-Efficiency Comparison: Figure 4 shows the comparison between the energy consumption per bit as a function of the data rate. The wireless link energy decreases monotonically as the data rate D_R increases, since the cost of the voltage-controlled oscillator and receiver power are amortized over larger data rates. Likewise, the wired link energy decreases *slightly* when increasing data rate from 1Gbps to 4Gbps due to low channel attenuation of the signal. However, the energy per bit starts increasing after 4Gbps, because the voltage swing needs to be increased to overcome the channel attenuation, and support the required data rate. We observe that the wireless communication becomes more energy efficient, when the data rate exceeds 4.1Gbps. The precise location of the cross-over point is a function of the transceiver and LVDS circuit design, interconnect parameters and the communication distance. However, the trends indicate that a wired or wireless data transmission may be more energy-efficient depending on the data rate requirements. This result shows a great potential for optimizing the communication energy-efficiency in FHE systems, since the data rate requirements are typically diverse as observed in NoCs. For instance, the data rate between the sensor hub and SoC in Figure 1 is typically low, while the memory and display interfaces are very demanding. Furthermore, memory traffic itself can show significant variations over time as a function of the workload. Consequently, a hybrid combination of wired and wireless transmission strategies can be designed to minimize the communication energy. Moreover, dynamic management techniques can be utilized to switch between wired and wireless interfaces, when the data rate requirement fluctuate over time.

IV. Potential Application Areas of FHE

Flexible devices can be worn, have arbitrary shapes to surround objects, and incorporate multiple functions. Moreover, combination with the CMOS technology enables integrated sensing, powerful computation and communication in a truly wearable form factor. Hence, FHE can help in transforming personalized computing by providing a systematic approach to design wearable systems and arbitrarily shaped objects, such as electronic patches. In particular, SoPs equipped with physiological, biochemical, and motion sensing capabilities can be used in wireless body area networks (WBANs), which interconnect a variety of sensing/actuating nodes in or on the body through an energy-aware wireless network [4].

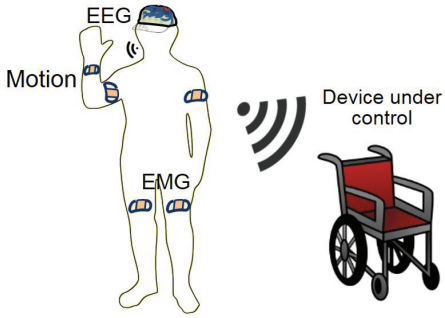

Fig. 5: Human machine communication using wearable SoPs.

A promising application of the FHE technology is in assistive IoT technologies [12, 21]. For example, FHE can be used to design electronic patches capable of motion processing and wireless communication. These patches can be placed to the arms and legs of the people suffering from movement disorders. Then, the movement of the patient can be analyzed *anytime* and *anywhere*. This is in stark contrast to the current practice, where a patient has to go to a clinic for examination. Likewise, this type of a patch can be used for gesture recognition, translating the sign language, and facilitating human-machine communication, as illustrated in Figure 5.

In addition to motion sensor patches, more complex systems such as a sensors for Electroencephalography (EEG) and Electromyography (EMG) signals can be made wearable, as shown in Figure 5. These sensors can enable wireless control of surrounding IoT devices like a wheel chair. The EEG and EMG sensor systems combine several stages: sensing, non-trivial processing of raw electrode signals, and communicating the user intent. Current solutions for processing requires a computer, while fully flexible technology lacks the computing power [2]. Thus, SoP designs can be suitably applied to these applications by combining the powerful rigid ICs for processing with the flexible lightweight form factor for wearable electronics.

To demonstrate the utility of the SoP concept, we developed a gesture recognition device with rigid ICs and thin Copper interconnects on a 25μm flexible Polyimide substrate, as shown in Figure 6. The device is capable of transmitting Gyroscope and Accelerometer data using a 2.4GHz inverted-F [36] patch

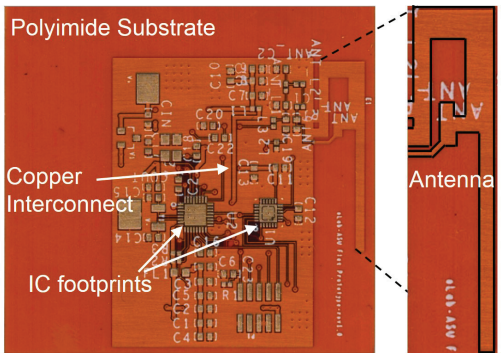

Fig. 6: A SoP prototype on a Polyimide substrate with zoomed antenna region.

antenna to another device with Bluetooth capability. Since the return loss of flexible antennas, such as a bow-tie antenna, may increase with bending [13], we also tested the flexible antenna on our prototype under different bending scenarios. We confirmed that the center frequency of our inverted-F antenna and characterized the received signal power as a function of bending. This shows promise for future inter- and intra-SoP connectivity using wireless transceivers.

V. Conclusion

Flexible hybrid electronics technology combines the advantages of traditional rigid ICs and printed electronics. Successful realization of a complete system capable of sensing, computation and communication can become possible with the advent of reliable, energy-efficient and high performance interconnect solutions. In this paper, we overviewed the communication challenges for FHE, discussed potential solutions, and presented promising application areas. Our preliminary results show that a wired link is preferred at low data rates, while wireless links become more energy-efficient when the data rate increases. Hence, a hybrid network of wired and wireless links can be designed as a function of specific bandwidth requirements.

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