NUMERO: 1655A - ANNO: 2015

A P P U N T I

STUDENTE: Piacibello

MATERIA: PowerElectronics + Eserc. Prof.Maddaleno

POWER ELECTRONICS

Franco Maddaleno

- "Alimentatori e commutazione", vol. II, part A, B (Politeko)
- "Power electronics", notes (course webpage)

classes
TUE 8:30
FRI 10:00

lab (not mandatory) LED 8
TUE 16:00

exam / written (eng) — 3 h max: close d book, theory
2 hrs.: open book, design
\ oral (eng)

30/09/2014

power elm → power threshold? No (may go from mW to MW)
↓ to distinguish it from signal elm

· it is power when dealing with EFFICIENCY
· converting electrical energy (electrical to electrical)

a. DC → DC
b. DC → AC
c. AC → DC
d. AC → AC

focus on

a. converter
b. inverter
c. rectifier
(d. cycloconverter, matrix converter)

d. not used any more
rather what is done is AC → DC → AC
rectifier | inverter
cost
better for performance
simplicity

Efficiency

$\eta = \frac{P_{out}}{P_{in}}$

P_{in} → [2] → P_{out}, P_d $\qquad \eta < 1$

→ increase η to decrease cost

→ $P_{in} - P_{out} = P_d > 0$ dissipated power (heat)

this relation is NOT instantaneous ($P_{in}(t) - P_{out}(t) > 0$)
because of power storage (⊣⊢)
but holds true for average: $\overline{P_{out}} - \overline{P_{in}} > 0$

Reason why we want high η:
① Heat dissipation
- temperature (T ↓ life ↑ : ΔT ≈ −10k brings about a DOUBLING of circuit life)

life grows exponentially with decreasing temperature
life $\propto 2^{-\Delta T}$

③ longer endurance (portable devices)

Suppose input power is not unlimited, or not as cheap as that one gets from mains

mains: ~ 20 cents per kWh
batteries: ~ 3 orders of magnitude larger !!

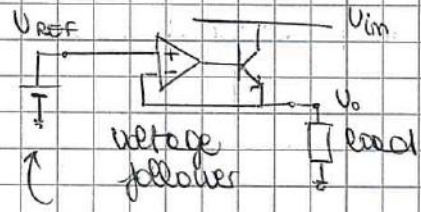
What was used in the past: linear regulators
(still used nowadays, but in specific cases/applications)

To get high efficiency: SWITCH MODE CONVERSION

Comparison:

LINEAR "POWER SUPPLY"

transistors are used as linear components



bandgap circuit — ✓ stable V_{REF} ✓ high I_{out}

(FAR)

power dissipation! $V_{CE} \cdot I_C$

$$V_F = \frac{V_o}{2}$$

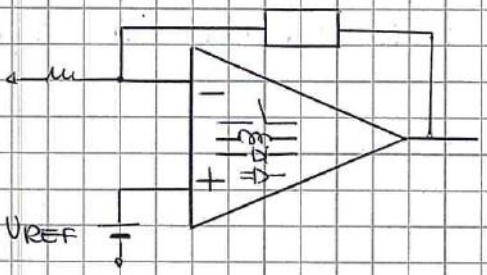
$$E_i = \frac{1}{2} V_o^2 C$$

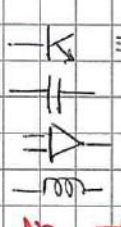
$$E_F = 2 \cdot \frac{1}{2} \left(\frac{V_o}{2}\right)^2 C = \frac{1}{4} V_o^2 C = \frac{E_i}{2}$$

whenever two $\frac{1}{4}$ are put in parallel, energy is wasted

SWITCH MODE CONVERSION

transistors can only be used as switches





ideally no dissipation!

(forced to use it)

NO — can be used because they dissipate power!

Basic steps

① BASIC TOPOLOGIES

② SMALL SIGNAL MODEL

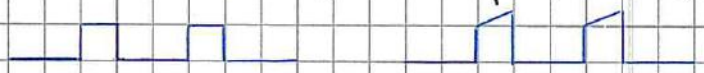
Why do we need it: because we need to know the transfer fun. of the system (circuit) to be controlled in order to close the loop around it and build the control / stabilize it!..

③ DERIVED CONVERTERS

① BASIC TOPOLOGIES

Families
(based on wave forms they work on)

a. Square wave (or trapezoidal) on voltage



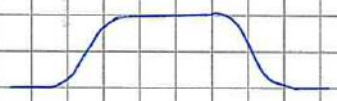
(piecewise linear)

focus on

b. quasi square wave (or resonant)

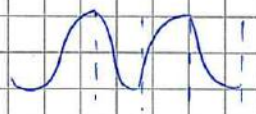
(edges are sinusoidal) ✓ smoother transition good for EMI

c. quasi resonant



- edges and some other parts of the wave form are sinusoidal
- linear far away from transitions

d. resonant



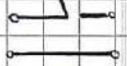
wave forms are piecewise sinusoidal, all of them with same frequency!

e. multi resonant

wave forms are piecewise sinusoidal where sinusoids have different frequencies!

Simplifying hypothesis

1. IDEAL SWITCHES (no losses)



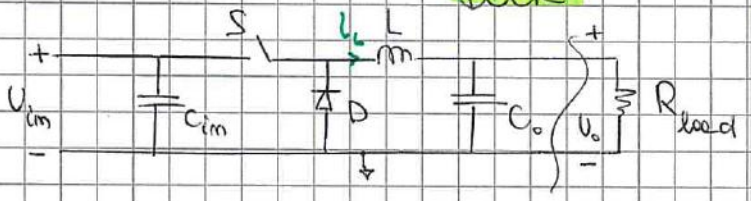
open $I = 0$
closed $V = 0$

2. RC and $\frac{L}{R}$ TIME CONSTANTS τ MUCH LARGER THAN SWITCHING PERIOD T_{sw}

$$\tau \gg T_{sw}$$

$\Rightarrow$ LINEAR WAVEFORMS (straight lines / no exponentials) RC, $\frac{L}{R}$ LC no more sinusoids)

BUCK



S can be:
- ✓ MOS
- ✓ IGBT
- ✓ BJT
- × not a thyristor (SCR) (diode that can be commanded to be turned on by a command terminal but turns off only when the current through it goes to 0 cannot be forced to switch off from the outside) because it will never turn off !!

D can be: an active diode
a switch (will see in the following)

R_{load}:
- not a true resistor
- modelled as a resistance because it absorbs power
- not part of the converter!

Modes of operation:

- CCM (Continuous Conduction Mode) $i_L \neq 0$ at all times $(i_L > 0)$

  better: $\frac{d}{dt} i_L \neq 0$

- DCM (Discontinuous Conduction Mode) $i_L = 0$ in part of the cycle

  better: $\frac{d}{dt} i_L = 0$

- circuit behaviour changes drastically from CCM to DCM (stable in one case, unstable in the other)
- design must enable to go from CCM to DCM without changing physical components!

Analysis

— m — $v_L = L \frac{di_L}{dt}$ $\quad \overline{v_L} = \overline{L \frac{di_L}{dt}} = L \frac{d\overline{i_L}}{dt}$

—||— $i_c = C \frac{dv_c}{dt}$

$\frac{V_o}{V_{im}} = \frac{T_{on}}{T_{on}+T_{off}} = \frac{T_{on}}{T_{sw}} = D$ according to assumptions

1. ideal switches
2. $\tau \gg T_{sw}$
3. no ripple
4. cyclostationary cond.

Notice: all of the assumptions have been used!

- 1. is easily removed: $V_{im} \to V_{im} - V_{sw}$ (done in the follow.) $0 \to -V_d$
- 2. is accurate enough and will never be removed

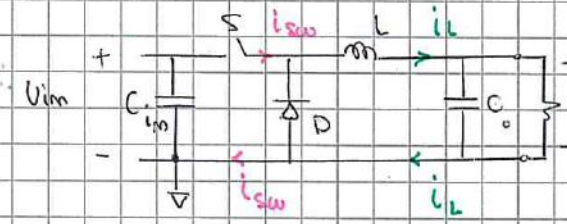
although the $i_L(t)$ wave form is not a ramp, but an exponential at best (due to $\frac{}{R}$ in series to $\frac{}{m}$) or even a sinusoid due to C_o kicking in if τ_{RL} and τ_{LC} are both $\gg T_{sw}$, the portion of wave forms we observe before switching, is so small that the linear approximation is very good

- 3. will be removed in the following
- 4. " " " " "

3/10/2014

Alternative Schematics for Buck converter (TOPOLOGICAL CHANGES only!)

Notice: the same current i_L → flowing through the inductor flows back into the bottom wire and the same i_{sw} → flows back in the wire below S as well.

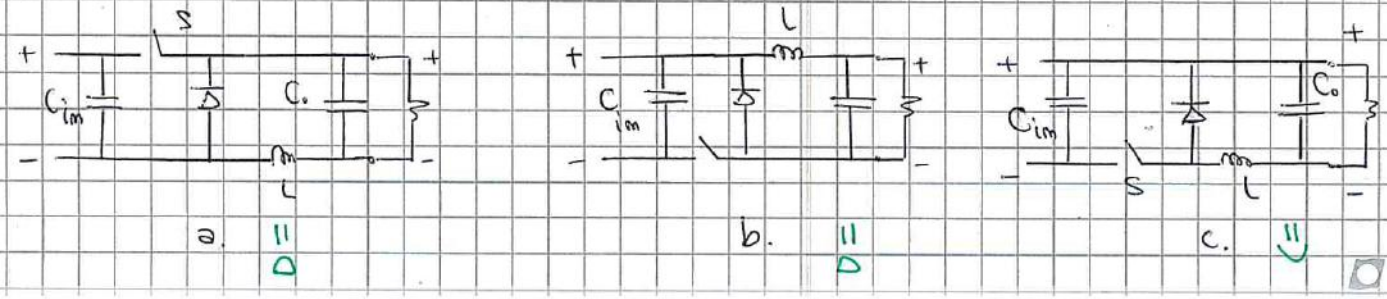


(d.)

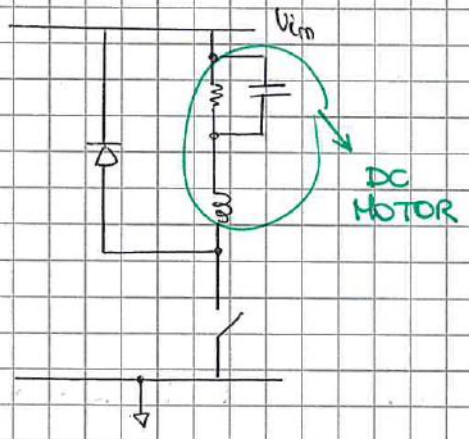
one could swap + - input nodes too: but then the diode has to be inverted and the switch changes type (npn → pnp)

- So $\frac{}{m}$ can be put in series to the RC output section either above or below (a.)
- Similarly $\frac{L}{S}$ can be either placed above or below (b.)
- we might as well move both $\frac{L}{S}$ and $\frac{}{m}$ at the same time (c.)

In all cases, the topology we get is a BUCK



Another configuration yet.



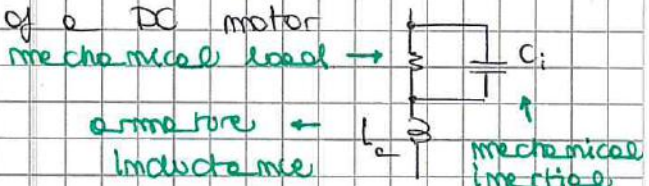
e.

Electrical engineers call it CHOPPER

(same as buck!)

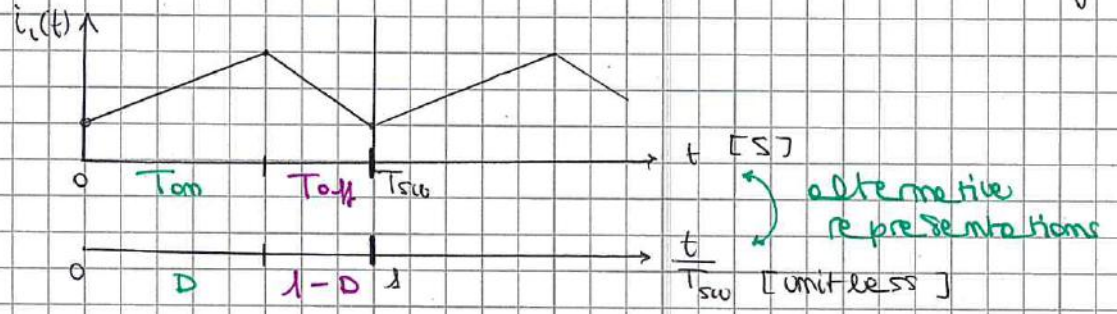
Still a buck, because:

- one side of $\frac{n}{L}$ is connected to a $\frac{1-D}{D}$ and a $\frac{1}{s}$
- the other side of $\frac{n}{L}$ is connected to the load ($\perp$) and output $\perp$
- the ◯ block is not made of discreet components, it is the model of a DC motor

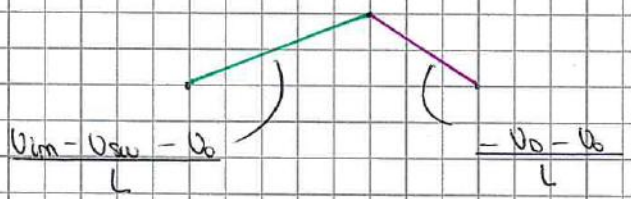


Remove hypothesis 1. (ideal switches)

- the waveform shape and qualitative behaviour stay the same



- but SLOPES CHANGE!



- and so the in-out equation changes as well: (but it is still found in the same way)

$$\frac{V_{in} - V_{sw} - V_o}{L} \cdot \frac{T_{on}}{T_{sw}} - \frac{V_D + V_o}{L} \cdot \frac{T_{off}}{T_{sw}} = 0$$

$$(V_{in} - V_{sw} - V_o)\, D - (V_D + V_o)(1 - D) = 0$$

$$\Rightarrow V_{o,real} = (V_{in} - V_{sw})\, D - V_D (1 - D)$$

recall $V_{o,ideal} = V_{in} \cdot D$

$\frac{\partial V_o}{\partial V_{in}}$: AUDIO SUSCEPTIBILITY

$\frac{\Delta V_o}{\Delta V_{in}}$: LINE REGULATION

$\frac{\partial V_o}{\partial D}$: GAIN

$\frac{\Delta V_o}{\Delta D}$: ? meaningless, never used

$\frac{\partial V_o}{\partial I_o}$: OUTPUT RESISTANCE

$\frac{\Delta V_o}{\Delta I_o}$: LOAD REGULATION

$\frac{\partial V_o}{\partial V_{in}}$, $\frac{\Delta V_o}{\Delta V_{in}}$: unitless

$\frac{\partial V_o}{\partial D}$: [V] units: Volt dimensions: voltage

$\frac{\partial V_o}{\partial I_o}$, $\frac{\Delta V_o}{\Delta I_o}$: [Ω]

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for a buck in CCM: $V_o = V_{in} \cdot D$

$\frac{\partial V_o}{\partial V_{in}} = D$ ↑

$\frac{\partial V_o}{\partial D} = V_{in}$ ↑ gain changes with input volt. like a parametric amplifier

$\frac{\partial V_o}{\partial I_o} = 0$ ↑ provided there are NO LOSSES!

if $\frac{R_L}{L} \neq \frac{R_L}{R_L}$ $\frac{\partial V_o}{\partial I_o} \neq 0$!

Introducing the notation:

$\frac{\partial V_o}{\partial V_{in}} \triangleq M$ for any converter, in any operating condition

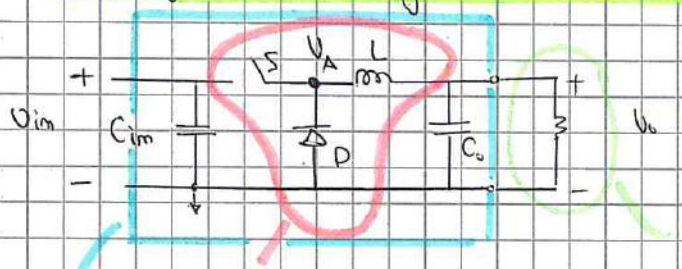
then, for the buck in CCM $M = D$ holds

Notice: $\frac{\partial V_o}{\partial I_o} = 0$ good or bad? WONDERFUL!

because the converter is almost like an ideal voltage source, i.e. zero output resistance

In general:
- all converter types are ≅ ideal voltage sources in CCM
- in DCM, converters have finite output resistance ↓ D

Waveform analysis: stresses and design choices



just a shorthand to indicate the load, not part of the converter

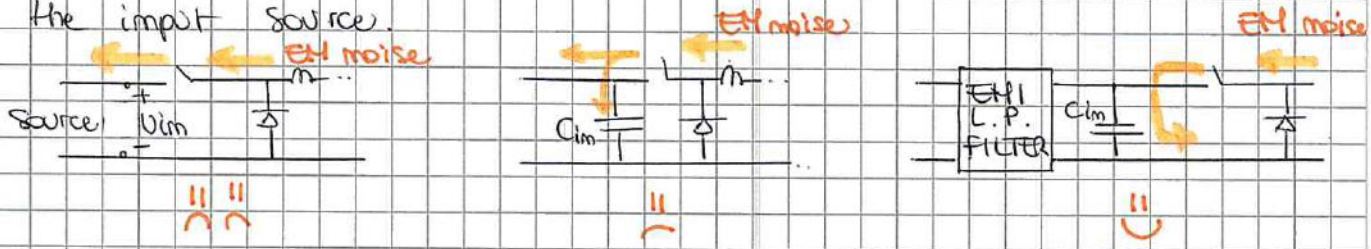
according some non-engineering book, the only components that make up the converters (no ≠)

↓

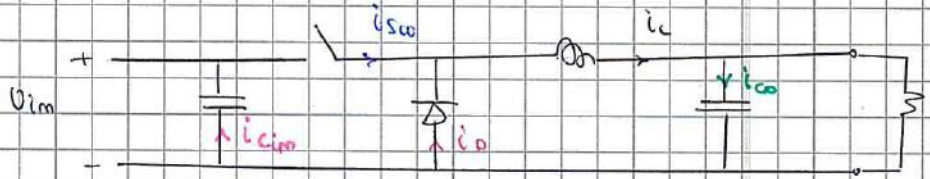
in fact, ≠ C_{in} and ≠ C_o are part of the converter as well!

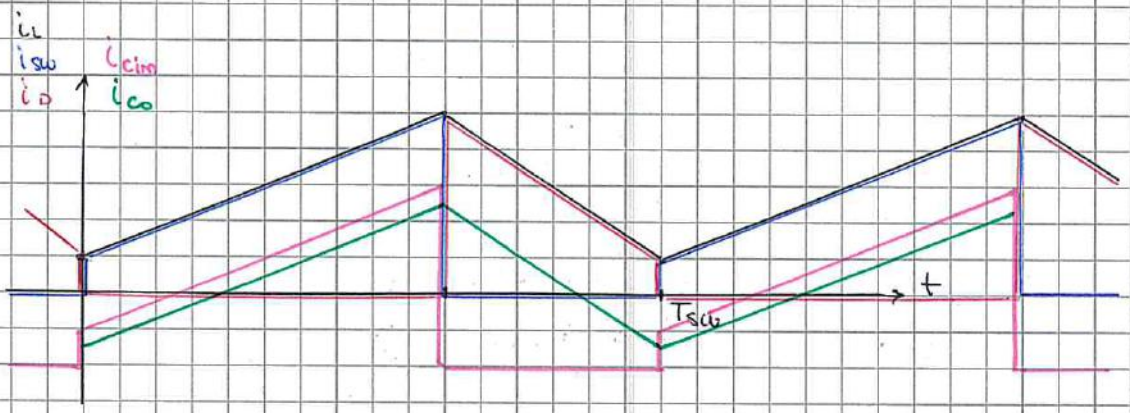
FILTER has to be placed at the input of the converter.

The ⊣⊢ Cin is part of the EMI FILTER and has the role of shorting the generated EM noise so that it doesn't reach the input source.



Despite ⊣⊢ Cin being part of the EMI filter, it is not designed by the EMI guys, but by the power elm. guys.





1) Switch current $i_s(t)$ ——

$i_s(t) = 0$ during T_{off}, when S is open
$i_s(t) = i_L(t)$ during T_{on}, when S is closed, because D is open so no current flows through it

2) diode current $i_D(t)$ ——

$i_D(t) = 0$ during T_{on}, when D is open
$i_D(t) = i_L(t)$ during T_{off}, has current through the inductor has to keep flowing and comes through S

3) current through output capacitor $i_{Co}(t)$ ——

if V_o = constant then $i_{Co}(t) = 0$ during all cycles

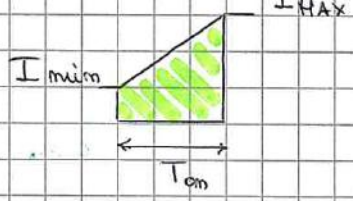
Stresses

- output: not very stressed, because i_{CO} is triangular (smooth enough, no jumps) and quite small
- input: very stressed, because i_{CI} is pulsed
  choice of $\frac{1}{n}$ C_{IM} is critical, based on the amount of current it can withstand (NOT the average, but the peak occurring at the pulse) and the RMS as well!

Example: computing averages (of periodic waveforms!)

- definition: $\tau = \frac{1}{T_{SW}} \int_0^{T_{SW}} i(\tau)\,d\tau = \frac{1}{T_{SW}} \int_{t_0}^{t_0+T_{SW}} i(\tau)\,d\tau \quad \forall t_0$
- graphically: area ◺ "spread uniformly" over a period, i.e. normalized by the period T_{SW}

– TRAPEZOID:

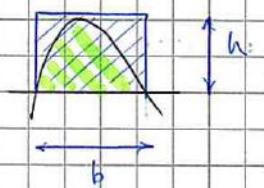


$$A = \frac{I_{MAX} + I_{MIN}}{2} T_{ON}$$

$$\tau = \frac{A}{T_{SW}} = \frac{I_{MAX} + I_{MIN}}{2} D$$

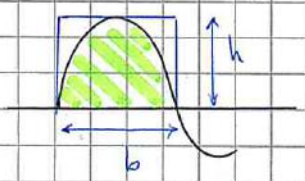
– PARABOLA:

$$A = \frac{2}{3} \cdot A_{\text{rectangle circumscribed}} = \frac{2}{3} b \cdot h$$



– SINUSOID:

$$A = \frac{2}{\pi} A_{\text{rectangle circumscribed}} = \frac{2}{\pi} b \cdot h$$



① $\frac{I_{MAX} + I_{min}}{2} = \frac{V_o}{R_L}$

② $I_{MAX} - I_{min} = \frac{V_o}{f_{sw} \cdot L}(1-D)$

→

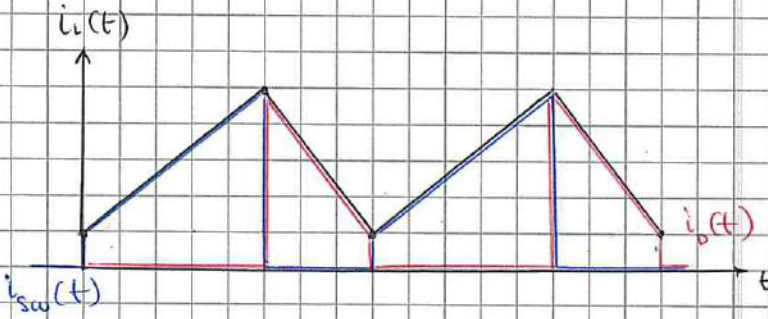
①+② $I_{MAX} = \frac{V_o}{R_L} + \frac{V_o(1-D)}{2 f_{sw} L}$ ($\frac{V_o}{R_L} = I_o$)

①-② $I_{min} = \frac{V_o}{R_L} - \frac{V_o(1-D)}{2 f_{sw} L}$

↑ analysis equations

↓ we need to get design equations in the end

I_o is typically a design constraint specified by the customer



(The only) design eqn. for a Buck (or even some converter derived from it)

$I_{min} > 0$ i.e. CCM operation

(in DCM we don't need it!)

$$I_{min} = \frac{V_o}{R_L} - \frac{V_o(1-D)}{2 f_{sw} L} > 0$$

CCM - DCM boundary: $I_{min} = 0 \Leftrightarrow \frac{1}{R_L} = \frac{1-D}{2 f_{sw} L}$

R_L: constraint (set by customer) just like I_o

D: not a degree of freedom, bcs for a Buck $D = \frac{V_o}{V_{in}}$ so it is fixed by constraints again

f_{sw}, L: degrees of freedom

typically f_{sw} is chosen (based on components / power level / technology / ..) and is derived after

#1 General rule: the higher the power, the lower the freq.

10 W	1 MHz → 300 kHz
100 W	500 kHz → 100 kHz
1 kW	100 kHz → 20 kHz

↑ for Buck only!

can always work below, but it is not convenient bcs L gets large

#2 General rule: if use BJT the f_{sw} has to be lower than it would be if MOS were used, bcs in BJT both majority and minority carriers are involved

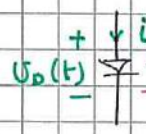
istantaneous power: $p(t) = v(t) \cdot i(t)$

↓ not really relevant for heating, bcs of thermal resist. (any object is like a LOW PASS FILTER for heat, so what matters is average power)

average power: $P_{ave} = \overline{p(t)} = \overline{v(t) \cdot i(t)} \neq \overline{v(t)} \cdot \overline{i(t)}$

$$P_{ave} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v(t) \cdot i(t)\, dt$$

- Example: POWER DIODE

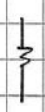


- when the diode is ON (conducting), the voltage drop across it is
  - almost constant → call it V_D
  - depending on technology
    - pin 1V
    - Schottky 0.5 V
    - SiC 2 V
    - Saturated BJT 1÷2V

$$P_{ave} = \frac{1}{T_{sw}} v_D \cdot I_{ave} \cdot T_{sw}$$

$$P_{ave} = v_D \cdot I_{ave}$$

- Example: RESISTOR



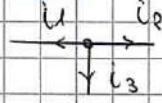
$$P_{ave} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v(t) \cdot i(t)\, dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} R\, i^2(t)\, dt =$$

take out

$$= R \cdot I^2_{RMS}$$

RMS current comes into play whenever coils/windings are involved (—ww—, —mm—) or even saturated MOS transistors (whose channel is resistive)

Beware: KCL $\sum_{node} i = 0$



what i should we use?

a. $i(t)$: instantaneous ✓ ok

b. $\overline{i(t)} = I_{ave}$: average?

$\overline{\sum_{node} i} = \overline{0}$ → $\sum_{node} \overline{i} = 0$ ✓ ok

linearity

I_{ave}

c. I_{RMS}? No $\sum I_{RMS} \neq 0$ because $I_{RMS} > 0$ and so the $\sum$ of positive numbers cannot be zero (i.e. RMS operator is not linear & so it cannot be exchanged with the average)

idea ↓

Consider $i(t) = I_{DC} + i_{AC}(t)$ ← fits well for representing $i_L(t)$, $i_{Lcim}(t)$, ...

where $\overline{i_{AC}(t)} = 0$ by def.

and compute its RMS value

Example: to check if the approximation is good

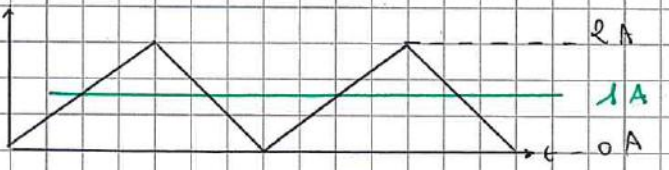
a.

$I_o = 1.9A$

$$I_{AC,RMS}^2 = \frac{\Delta i_L^2}{12} = \frac{(0.2A)^2}{12} \Rightarrow I_{AC,RMS} = \frac{0.2A}{\sqrt{12}} \simeq 57\,mA$$

$$I_{L,RMS} = \sqrt{I_o^2 + \frac{\Delta i_L^2}{12}} = 1.90003\,A \simeq I_o$$

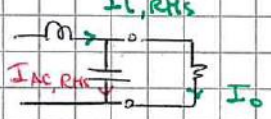
b.



$I_o = 1\,A$

$I_{L,RMS} = \sqrt{1 + \frac{1}{3}}\,A$

Question: suppose $I_{L,RMS}$, I_o are known. Can one find $I_{AC,RMS}$?



YES for mathematicians: because it just boils down to inverting an equation

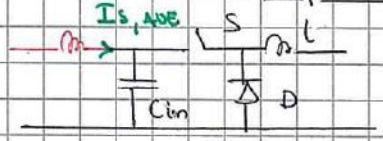
$$I_{AC,RMS} = \sqrt{I_{L,RMS}^2 - I_o^2}$$

NO for engineers: because of numerical cancellation

since $I_{L,RMS} \simeq I_o \Rightarrow I_{AC,RMS}$ would be just numerical noise!

Quadratic KCL can be effectively used to find AC current in sections carrying pulsating current!

Consider the input section of a buck in CCM



$I_{s,AVE} = I_{in}$

$$I_{s,AVE} = \frac{A_{trapezoid}}{T_{sw}} = \frac{(B+b)h}{2}\cdot\frac{1}{T_{sw}} = \frac{B+b}{2}\cdot\frac{T_{on}}{T_{sw}}\,D$$

$$I_{s,AVE} = \frac{I_{min} + I_{MAX}}{2}\,D = I_o \cdot D = I_{in}$$

(Once I_{in} has been estimated, input power can be evaluated)

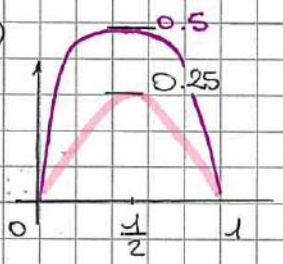
why we need $I_{s,RMS}$: to find $P_{diss,in} = \frac{1}{5}$ if it is a MOS, whose channel behaves like a resistor in saturation

Still need to find $I_{s,AC\,RMS} = I_{cin,RMS}$:

by quadratic KCL: $I_{cin,RMS} = \sqrt{I_{s,RMS}^2 - I_{s,DC}^2}$ No numerical cancellation!

$= \sqrt{I_0^2 \cdot D - I_0^2 D^2} = I_0 \sqrt{D - D^2} = I_0 \sqrt{D(1-D)}$

parabola parameter $\frac{1}{8}$ — $D(1-D)$ — $\sqrt{D(1-D)}$



worst case is

$I_{cin,RMS} = \frac{I_0}{2}$ and it occurs for $D = \frac{1}{2}$

$\Rightarrow$ input capacitor is heavily stressed

Example (the one used before): $I_0 = 1.9\,A$, $\Delta i_L = 0.2\,A$

$I_{co,RMS} = \frac{\Delta i_L}{\sqrt{12}} = 57\,mA$

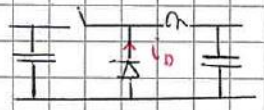
$I_{cin,RMS} \simeq \frac{1}{2} I_0 = 0.95\,A$!!

very heavy stress — compared to not any capacitor commercially in that

↓ more precise (still flat-top)

$I_{cin,RMS} \simeq 1.9\,A \cdot \sqrt{0.3 \cdot 0.7} = 0.87\,A$

Diode stresses



$\bar{i}_D = I_{D,AVE} = \frac{I_{MAX} + I_{min}}{2}(1-D) = I_0(1-D)$

$I_{D,RMS} = I_0 \cdot \sqrt{1-D}$ [flat-top approx.]

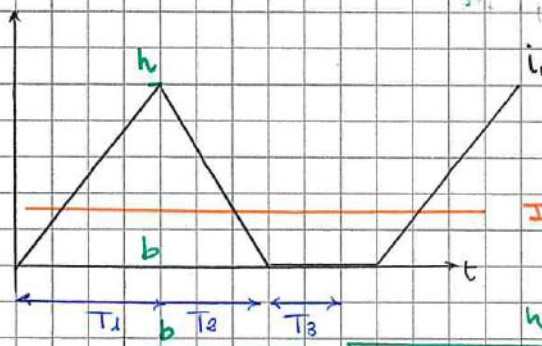
↑ USELESS (although correct) bcs for diodes we don't care of RMS stresses

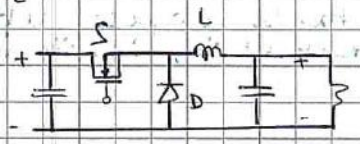
Beware: flat-top approx. is an approx. only for RMS; for averages it is exact!

10/10/2019

Since we have an extra unknown (T_2) we need an extra equation:

it is customary to use the relation between output current I_o and inductor current i_L





during T_3 neither S nor D is conducting and the left-hand node of L is left hanging, floating

$$\begin{cases} I_o = \dfrac{(T_1+T_2)\cdot\dfrac{V_{im}-V_o}{L}\cdot T_1}{2T_{sw}} = \dfrac{V_o}{R} \\ M = \dfrac{V_o}{V_{im}} = \dfrac{T_1}{T_1+T_2} \end{cases}$$

I_o is the average (DC) value of i_L:

$I_o = \dfrac{\text{Area triangle}}{T_{sw}}$

derive T_1+T_2 and substitute in $I_o = \dots$

Beware: it is no longer true that $\frac{T_2}{T_{sw}} = 1-D$ but it is still true that $\frac{T_1}{T_{sw}} = D$

$$\frac{V_o}{R} = D\,\frac{V_{im}-V_o}{2L}\cdot\frac{V_{im}}{V_o}\cdot\frac{T_1}{T_{sw}}\,f_{sw} =$$

$D \cdot D$

$$= D^2\,\frac{V_{im}-V_o}{2f_{sw}L}\cdot\frac{V_{im}}{V_o} \qquad \text{where } \frac{V_{im}}{V_o} = \frac{1}{M} = \alpha$$

$$\frac{1}{R} = \frac{D^2}{2f_{sw}L}\,\alpha(\alpha-1) \rightarrow \frac{D^2R}{2f_{sw}L}\cdot\alpha\cdot(\alpha-1) - 1 = 0$$

$$\alpha^2 - \alpha - \frac{2f_{sw}L}{D^2R} = 0$$

Observations:

- $\alpha(f_{sw})$ and $\alpha(L)$ are not a problem
- $\alpha(D)$: good 👍 it means V_o can be controlled varying D (topologies where M is not a fn. of D are useless!!)
- $\alpha(R)$: bad !! if the load changes, V_o changes (we don't have an ideal voltage source like in CCM)

$$\alpha = \frac{1 \pm \sqrt{1+\dfrac{8f_{sw}L}{D^2R}}}{2} = \frac{V_{im}}{V_o}$$

we have to use the + sign because we know that V_o, V_{im} have the same polarity in a buck

$$M = \frac{V_o}{V_{im}} = \frac{2}{1+\sqrt{1+\dfrac{8f_{sw}L}{D^2R}}}$$

So in DCM we can choose a smaller L (i.e. L_c is a lower bound for CCM and an upper bound for DCM instead) and $L_{c,DCM} < L_{c,CCM} \Rightarrow L_{DCM} < L_{CCM}$

but a smaller inductor is not really an advantage given the high current peaks that develop in all components!

Reason why one may be forced to work in DCM:

related to the controller one has to design and put in feedback around the converter to control V_o

↳ there are cases: when the converter in DCM is stable (or may be stabilized?) whereas in CCM it is unstable

(not so for the Buck, but see later Boost and Buck-boost)

↓

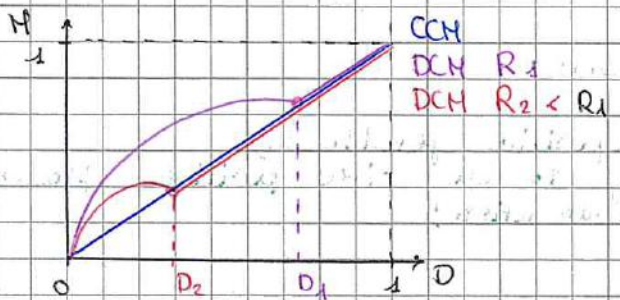
when we are forced to work in DCM by stability issues, we can't have very high powers converters because of the high current peaks

Comparison CCM - DCM

$$M_{DCM} = \frac{2}{1 + \sqrt{1 + \frac{8 f_{sw} L}{D^2 R}}} = \text{(derived under the 4 assumptions.. it will be slightly lower in the real case, with losses)}$$

$$M_{CCM} = D \quad \text{——}$$

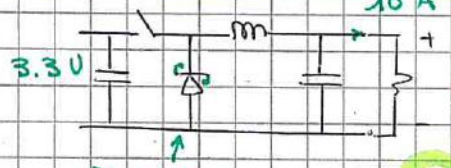
- in CCM we have one curve only, and it is a straight line (quadrants I, III bisettrix)
- in DCM we have a family of curves, each relative to a different load R, and M is larger than in CCM for a given D



- given a load R, the system is initially in DCM (unless designed otherwise) but eventually will go in CCM as D is increased. [point where the — curve joins the — one] After that if one further increases D it will stay in CCM, so — and — curves coincide.
- the point • is found solving $M_{DCM} = M_{CCM}$, i.e. $\frac{2}{1 + \sqrt{1 + \frac{8 f_{sw} L}{D^2 R}}} = D$
- the boundary btw DCM and CCM is $L_c = \frac{R(1-D)}{2 f_{sw}}$ and once L and R are fixed one can solve for D. If for R_1 the boundary is D_1, for $R_2 < R_1$ the boundary will be $D_2 < D_1$

(for R very small, one is in CCM for any value of D)

Low - V, high - I buck : efficiency and diode choice



a.

$D = \frac{1V}{3.3V} = 0.3$ (in the ideal case of no drop over -|t|-)

$1 - D = 0.7$

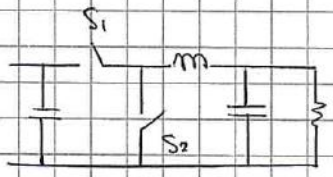
$P_o = 10A \cdot 1V = 10W$

$P_{D,d}$? $P_{S,d}$? power dissipated by D, S when they are on

3.3V level : typical of logic circuits (pc motherboards)

- we design the Buck to work in CCM, i.e. to have

- the drop over the diode causes a large error because it is comparable to the output voltage level (even if we choose a Schottky diode rather than a standard pin, which is the good choice for such low voltage levels)
  - during T_{off} the diode conducts 10 A & drops 0.5V, so it dissipates 5 W
  - during T_{on} the MOS switch conducts 10 A & drops 0.1V, so it dissipates 1W
  - ⇒ especially due to -|t|-, η is low !!



b.

b. is more expensive than a. for 2 reasons:
- S_2 (MOS) is more expensive than D (diode)
- extra circuitry is needed to drive S_2 (unlike the diode, which is driven by V, I in the circuit itself)

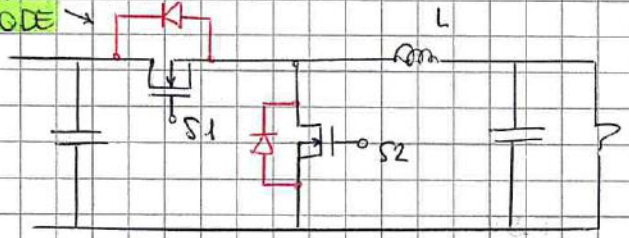
⇒ if S_1 is on during D, S_2 is driven with "$\bar{D}$" i.e. is off when S_2 is off and vice versa

Solution b. is an improvement that increases η because it gets rid of -|t|- which is the main problem : we want to replace it with a switch whose V_{on} is $\ll 0.5$ V
(no diode can do that, we have to use a MOS)

	η	COST
a.	=	=
b.	=	=

Driving signals

BODY DIODE



problem: if S_1, S_2 are both closed there is a short circuit that kills the switches

problem: (bcs i_L doesn't stop) if S_1, S_2 are both open V_A goes to a very high negative value and kills the switches

↓

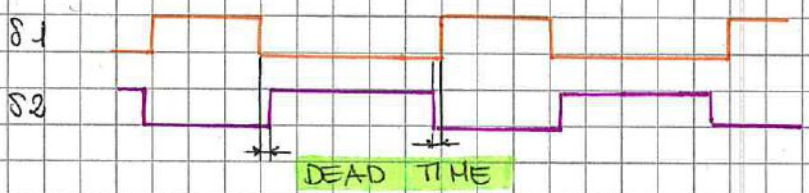
it would seem that it doesn't work

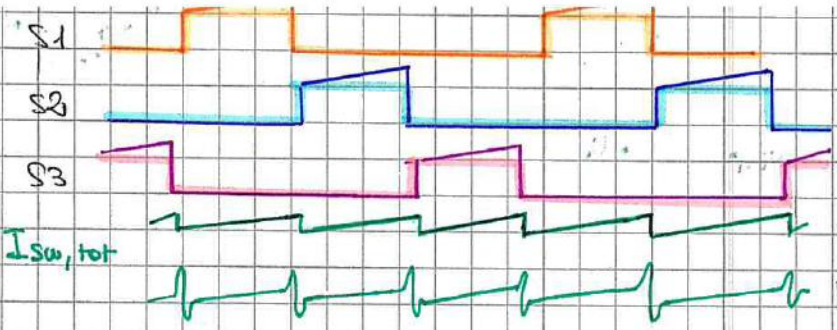
↓

IN FACT IT WORKS provided that the scheme is changed and the driving signals are slightly modified as such

SYNCHRONOUS BUCK

c.





a. is in case D = 30 % exactly and the 3 switches are never conducting at the same time

b. is in case D is slightly larger than 30 % and 2 switches are conducting both, for a short time: peaks are $\simeq 2 I_o$ (60 A if each converter has 30 A output)

The good points are that:

- each component has to carry 1/3 of the average desired I_o, which is very high (90 A)

but in particular

- the RMS component of $I_{sw,tot}$ is very low

(i.e. the duty cycle that Cin sees is just the overlap btw the driving signals - that is the width of the current peak - ⇒ very small, ~ 3 % or so)

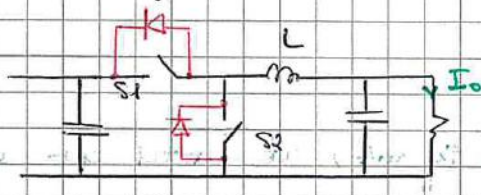
- the RMS component of I_{co} too

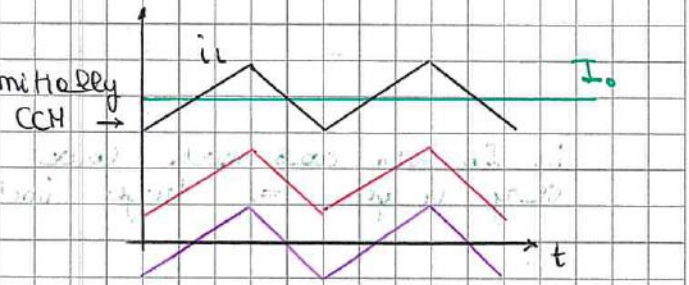
It is called MULTI PHASE CONVERTER

14/10/2014

Synchronous converter:

- works the mos to the ⊣⊢ in parallel to ⏦
- if ⏦ is a MOS, the body diode is there due to the tech. process itself
- if ⏦ is a IGBT, the diode is not there for free but it is put there by the manufacturer (in the same package of the IGBT switch)
- what if I_o decreases?

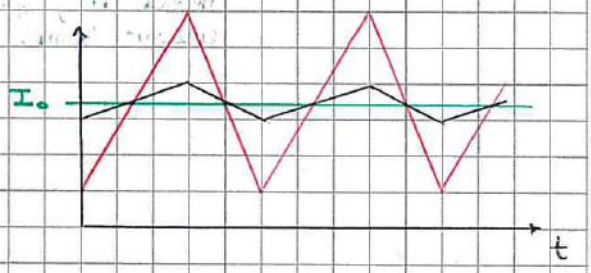




the average of i_L decreases
but its ripple stays the same
if the volts don't change.
Progressively decreasing I_o: — still CCM ⇝ — still CCM!
because i_L goes to 0 but does not remain to 0, it goes < 0
i.e. starts flowing backwards!
In fact, during T_{off} S2 is closed so $\frac{L}{m}$ has 0 V to its left-hand terminal and V_o to its right-hand

b. if Δi_L is very large (i.e. L is small and cheap) we save money with L but cost increases significantly due to the very strong stress all the components are subject to.

if $I_{o,min}$ is not given one commonly assume it is 0, because to stay in CCM an ∞ L would be required



CCM operation can only be ensured above a given $I_{o,min}$, for which a reasonable value is

$$I_{o,min} \simeq \frac{I_{o,MAX}}{10}$$

because it ensures for L a reasonable value, and for Δi_L too

- critical inductance: $L_c = \dfrac{(1-0.43)24\,\Omega}{2 \cdot 200\,kHz} = 35\,\mu H$

  to account for tolerances (to be safe)! : increase by 10% and choose a normalized value close to $40\,\mu H$: $L = 39\,\mu H$

  (may choose 47 µH as well : it is likely to be a bit more expensive but it is a safer choice. With 39 µH it may happen that we go in DCM close to $I_{o,min}$, but it is no big deal because that just depends on an arbitrary choice of $I_{o,min}$: it is enough to rise it a little if needed)

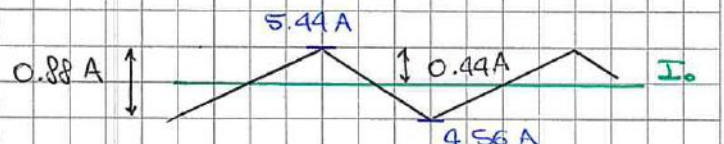
- current ripple: $\Delta i_L = \dfrac{v_o}{L} \cdot \dfrac{(1-D_{min})}{f_{sw}} = \dfrac{12V\,(+v_o)\,(1-0.43)}{39\,\mu H \cdot 200\,kHz} =$

  ↓ it is the largest there can be! May be less if $V_{in}\uparrow$ $D\uparrow$

  $= 0.88\,A$ (peak to peak)

  Check: $I_{o,min} - \dfrac{\Delta i_L}{2} =$

  $= I_{L,min} = 60\,mA > 0$



we picked the right L !! => we stay always in CCM, although we go very close to the DCM limit

- Notice: imposing CCM just fixes L. All other design constraints are given by the STRESSES

- parameters to choose an inductor

  nominal value: $L = 39\,\mu H$
  peak current: $I_{L,max} = 5.44\,A \rightarrow 5.5\,A$ (saturation)
  RMS current: $I_{L,RMS} \simeq I_{L,DC} = I_o = 5\,A$ (losses)
  switching freq: f_{sw} ↑ good approx. worth using

we now need $D_{max} = \frac{V_o}{V_{in,min}} = 0.6$ to evaluate worst case

$I_{S,RMS} = I_o \cdot \sqrt{D} = 5A \cdot \sqrt{0.6} = 3.9\,A$

$I_{S,peak} = I_{L,max} = 5.94\,A$

$I_{S,ave} = I_o \cdot D_{max} = 5A \cdot 0.6 = 3A$

reason why it is good practice to evaluate it:

to estimate P_{in} and so η: we should get $P_{in} \gtrsim P_o$

- not exactly $P_{in} = P_o$ because $\eta = 1$ is really possible
- if we got $P_{in} < P_o$ there is clearly some mistake
- if we got $P_{in} \gg P_o$ we would be very bad engineers :D

$I_{S,ave} = I_{in} \Rightarrow P_{in} = I_{in} \cdot V_{in,min}$

where $V_{in,min}$ is used because it corresponds to D_{max}, which was used to evaluate I_{in}

$P_{in} = 3A \cdot 20V = 60\,W$ ✓ reasonable since we are assuming no losses

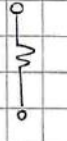
$P_o = V_o I_{o,MAX} = 60\,W$

in fact P_{in} will be $> 60\,W$ because $D_{max} > 0.6$, due to losses!

maximum voltage stress on the switch (when off!):

$V_{DS,max} \simeq V_{in} = 28\,V$ (+ $V_{D,on}$) ⟶ reasonably, pick $\sim 40\,V$

This is not enough to pick a MOS: important parameters are

- $V_{DS,max}$: (also referred to as $V_{BR\,DSS}$) breakdown D to S voltage when G is shorted to S
- $V_{DS,on}$:  $V_{DS,on}$ — the channel of the MOS when on, is like a resistance $R_{DS,on}$ across which a voltage $V_{DS,on}$ drops

(actually $R_{DS,on}$ has to be specified)

Once $V_{DS,on}$ and $I_{S,RMS}$ are known, power dissipation is evaluated as

$P_{SW} = R_{DS,on} \cdot (I_{S,RMS})^2$

Beware: it can't be summed up to P_D of the diode because they refer to different conditions (D_{min}, D_{max})

On the market, one can find some 40 V parts but many more 55 V (very common bcs it is the minimum requirement for automotive applications): both are ok in our case, just don't go as low as 30 V.

Summary of parameters

MOS $V_{BR\,DSS} = 40\,V$ (55 V) ← those to look for on the data sheet

$r_{DS\,on,HOT} = 37\,m\Omega$ ← that to be used to evaluate

$r_{DS\,on\,COLD} = 20\,m\Omega$ ← those to look for on the data sheet

Power dissipated by MOS (not all of it!) but most of it

$$P_{d,s} = r_{DS\,on} \cdot I^2_{s,RMS} = 37\,m\Omega \cdot (3.9\,A)^2 = 0.56\,W$$

(Mind the difference btw $r_{DS\,on}$ hot and cold:
- look for cold on the data sheet, not to be tricked
- use hot to evaluate P_d)

- choice of input capacitor C_{in}

1 – working voltage: > V_{in}

R5 Series: 10 16 25 40 63

reasonable to pick $V_w \simeq 40\,V$

2 – RMS current:

$$I_{cin,RMS} \geq I_o \sqrt{D(1-D)} =$$ ← flat-top approx.

in this case the worst case is given by $D = 0.5$ (top of the parabola)

$$= 5\,A \cdot \sqrt{0.5^2} = 2.5\,A$$ very high stress !!

3 – capacitance value? DON'T REALLY CARE

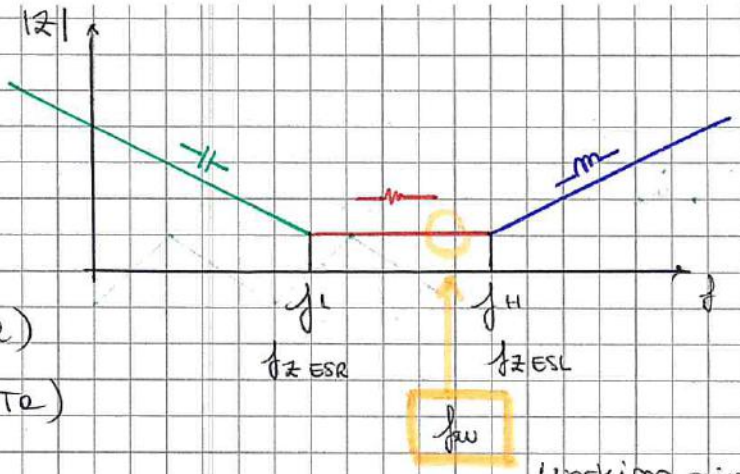
because C_{in} is not enough to keep impulsive current from entering the source by itself, a input LP EMI filter will be needed ⇒ the overall impedance will be modified, so we don't care much

⇒ pick the smallest value of C_{in} that has the required
- V_w
- $I_{cin,RMS}$

4 – technology? have a fixed polarity!

2. ELECTROLYTICS / Al
Ta

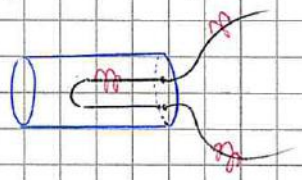
a. ELECTROLYTIC



f_L : 1 kHz ÷ 10 kHz (Al) / 10 kHz ÷ 50 kHz (Ta)

f_H ~ MHz but it is hard to define because it is affected by PCB traces too (ESL given by the data sheet is only the inner part of the capacitor, then one should account for all of the output circuitry)

Working point of the switching converter



~ 1 µH/mm

$f_L = f_{Z\,ESR} = \frac{1}{2\pi C \cdot ESR}$ where $ESR = \frac{V_{o,ripple}}{I_{o\,ripple}} = \frac{100\,mV}{0.88\,A} = 113\,m\Omega$ (Ohm's law: $I_{o\,ripple} \uparrow \Delta i_L$)

(NOT to be normalized bcs it is parasitic!)

design constraint:

⇒ we have to look for ESR < 113 mΩ to have $V_{o,ripple}$ < 100 mV

Rough estimate of value of C_o:

$C_o = \frac{1}{2\pi f_{Z\,ESR} ESR} \simeq \frac{1}{2\pi \cdot 110\,m\Omega \cdot 3\,kHz} \simeq 0.5\,mF$

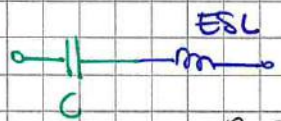
↑ guess: 1 ÷ 5 kHz

This has to be normalized: $C_o \simeq 470\,\mu F$

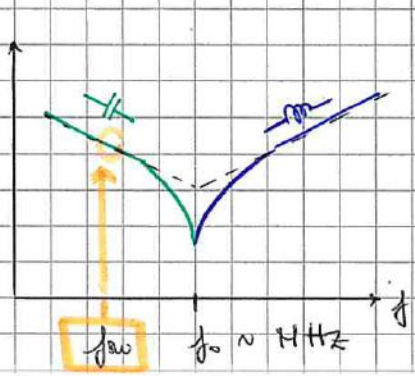
and will be needed to design the CONTROLLER

b./c. CERAMIC & FILM

- they have a negligible ESR ☺
- they have a relevant ESL



RESONANT CIRCUIT



– – : asymptotic Bode diag

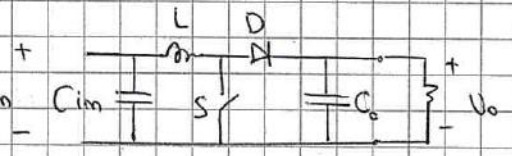
17/10/2014

BOOST CONVERTER

- $\frac{V_o}{V_{in}} \geq 1$: (step-up converter) "good point"

(one needs a switching circuit to go up in DC voltage, whereas to go down like in a buck is not that big a deal → may be done with transistors, resistors too)

- needs a controller in feedback to stabilize it "bad point"



C_o this time has to be there, it is part of the converter, unlike in the buck, in which it is just convenient to have it to make the LP output filter II order

- compare buck and boost topologies:
  - C_{in} is not really part of the Boost converter it is just there to avoid exporting EM noise to the source
  - C_o is a part of the Boost converter, has to be there
  - one may get from one topology to the other just by "rotating" the L, D, S elements

  - inductor at the input:

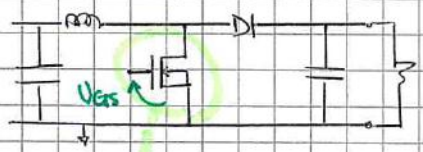
since the i_L is typically quite smooth (not pulsating, just a small ripple, small AC component) the input capacitor is not very stressed and L protects from input overvoltages D and S

(unlike in the buck!)

  - low side switch, easier and less expensive to drive than high side switch ↑

the one we have in the buck!

(it is high side both if it is a nMOS or a pMOS)



LOW SIDE

(source connected to reference pot.)

A MOS is controlled by its V_{GS} voltage: if the S is not at a fixed potential (↓) but swings (e.g. from 0 to V_b) between different potentials depending on the phase (Ton or Toff), the G voltage has to "follow" to drive it properly.

More difficult and more expensive driving. "

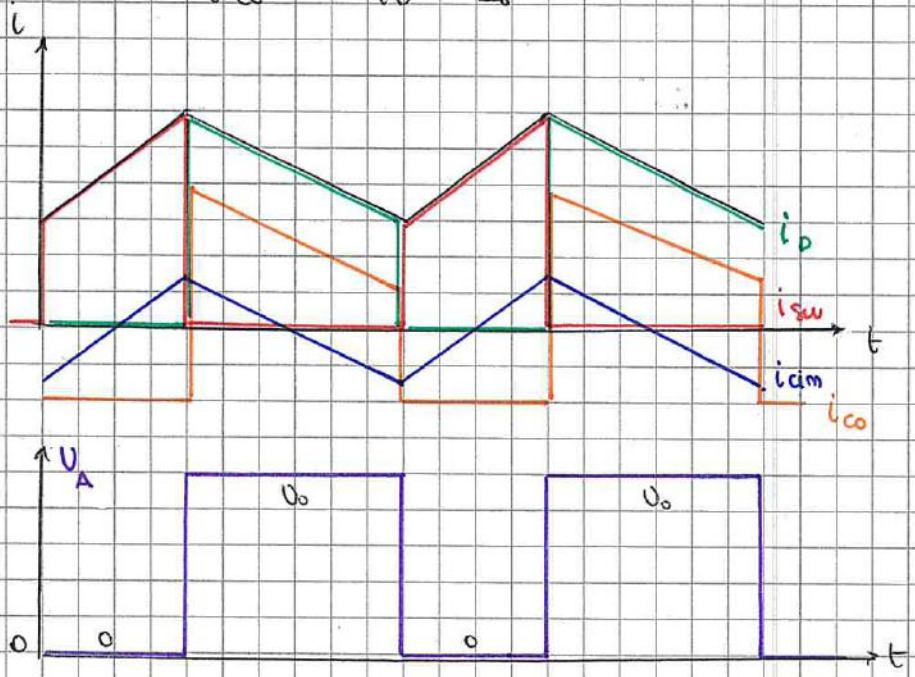
If instead S is at a fixed potential (↓) as in the Boost, one just needs to drive the G voltage above V_{th} (Ton) and below V_{th} (Toff), without changing the "floor" voltage level.

If we want to account for losses: $\frac{V_{in} - V_{sw}}{L}$ $\qquad$ $\frac{V_{in} - V_o - V_o}{L}$

(actually there is still the drop on parasitic resistance of the inductor)

Once we know i_L we can find all the other waveforms in the circuit:

- $i_{sw} = \begin{cases} i_L & \text{during } T_{on} \\ 0 & \text{during } T_{off} \end{cases}$
- $i_D = \begin{cases} 0 & \text{during } T_{on} \\ i_L & \text{during } T_{off} \end{cases}$
- $i_{cin} = i_L - \overline{i_L}$
- $i_{Co} = i_D - I_o$



Notice:

a. the shape of i_D and i_{sw} (and i_L!) is the same for all topologies (Buck, Boost, Buck – boost), although slopes change

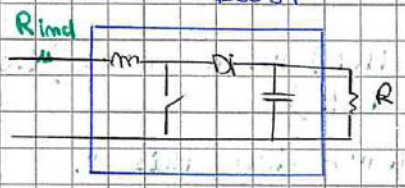
b. what changes from one topology to another is the shape of i_{cin} and i_{Co}

c. to be precise, we can't say what i_{cin} is until we specify which is the source. If it was an ideal DC voltage source, i_{cin} would be 0. But we know it is not, because at the input there are L, Cs that make up the EMI filter, so we can say that in Cin all the i_L ripple flows ("by design")

d. input and output capacitor currents of the Boost are just swapped with the Buck

Cin:	pulsating	smooth
Co:	smooth	pulsating
	Buck	Boost

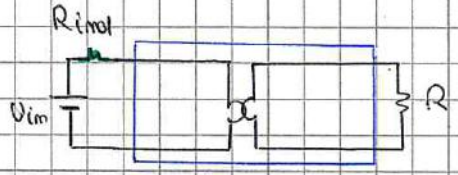
BOOST



$V_o = V_{in} \frac{1}{1-D}$ (just proved)

$I_o = I_{in}(1-D)$ (power conservation)

$1 : \frac{1}{1-D}$ TRANSFORMER : step-up DC transformer



EQUIVALENT CIRCUIT

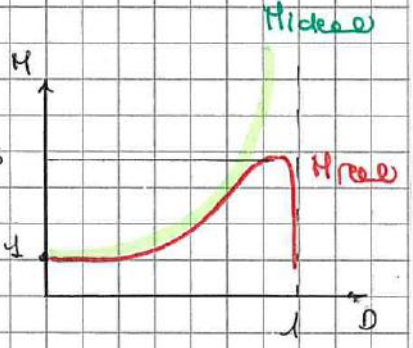
BUT ideal components do not exist!

Let us consider just one parasitic element: the wire resistance of the inductor — Rind

The equivalent circuit has:
- an ideal voltage source
- a series resistance
- an ideal transformer, with turn ratio $\frac{1}{1-D}$, that is somehow "magic" because it can transform DC
- a load (resistive)

If we keep all idealities but Rind and compute $V_o(D)$, we find out that it doesn't go to ∞ anymore.

The actual behaviour shows a saturation for some value of D and a decrease of V_o if D is further increased beyond such a value.



(It was enough to consider one non ideality to spoil the ideal behaviour)

The efficiency @ the maximum is $\eta = \frac{1}{2}$ (condition for power matching)

We use the ideal expression for H because we work for D small enough that losses are not so relevant.

CCM / DCM boundary

$$I_{min}=0 = \frac{V_o}{R(1-D)} - \frac{D(1-D)V_o}{2 f_{sw} L}$$

f_{sw} : degree of freedom (1st choice during design)

D : constraint (from specs on V_{in}, V_o)

$$D = \frac{M-1}{M} \quad \text{where} \quad M = \frac{V_o}{V_i}$$

R : constraint (from specs of I_o, V_o)

$$R = \frac{V_o}{I_o}$$

L : degree of freedom (derive it based on previous choice of f_{sw})

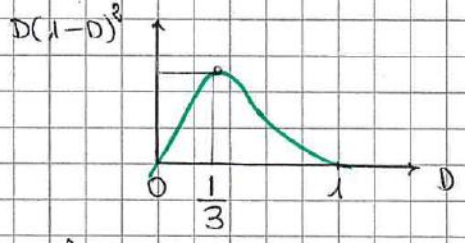
$$\Rightarrow \quad L_c = \frac{D(1-D)^2 R}{2 f_{sw}}$$

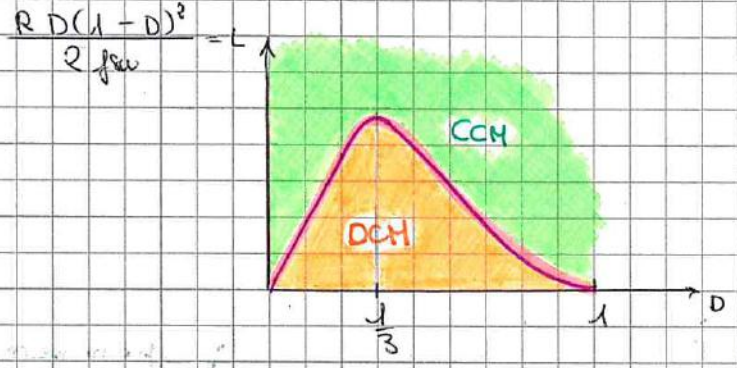
$L > L_c$ CCM
$L < L_c$ DCM
} considering worst case for each!

Worst cases?

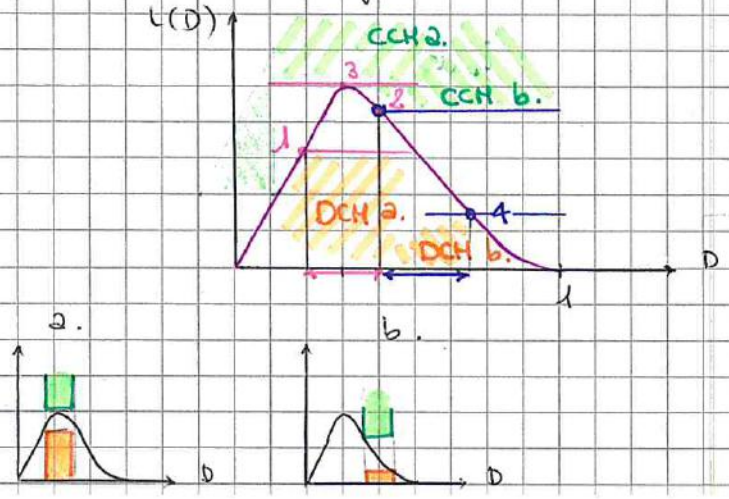
CCM : $\max(R) = R_{max}$

$\max(D(1-D)^2) = D(1-D)^2 \Big|_{D=\frac{1}{3}}$: the worst case occurs neither for $D_{min}=0$ nor for $D_{max}=1$, because the function is not monotonic





Example : determining worst case D



a. given a D in the — range

CCM above point 3
DCM below point 1

b. given D in the — range

CCM above point 2
DCM below point 4

Derive T_2 from equation 4:

$$T_2 = \frac{T_1}{M-1}$$

$$\Rightarrow \text{eq. 2} \quad \frac{M}{R} = \frac{1}{2}\cdot\frac{D}{L}\cdot\frac{T_1}{M-1}$$

$$M(M-1) = \frac{1}{2} R \frac{D^2}{L f_{sw}} \quad \leftrightarrow \quad M^2 - M - \frac{RD^2}{2L f_{sw}} = 0$$

$$M = \frac{1 \pm \sqrt{1 + \frac{2RD^2}{L f_{sw}}}}{2}$$

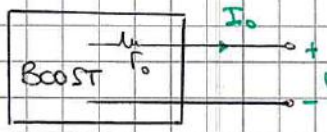
sign − is unphysical (because yields $M<0$)

- M depends on D: it is supposed to, we like that (even if not linear)
- M " " L, f_{sw}: not a problem, they are ≃ constant
- M " " R: don't like it much, bcs we don't have an ideal voltage source, but always happens so in DCM

Converter parameters for a DCM BOOST

- $\frac{\partial V_o}{\partial V_{in}} = M$ (makes sense: if we don't supply any V_{in}, we don't get any V_o)
- $\frac{\partial V_o}{\partial I_o} \neq 0$, in particular $\frac{\partial V_o}{\partial I_o} < 0$ negative output resistance

↑ because $M = M(R)$ where $R = \frac{V_o}{I_o}$



↑ related to sign convention

convention bcs converter is a source for the load, but r_o is a load from the point of view of the converter, so we get it $r_o<0$ unless we change convention

we use source sign

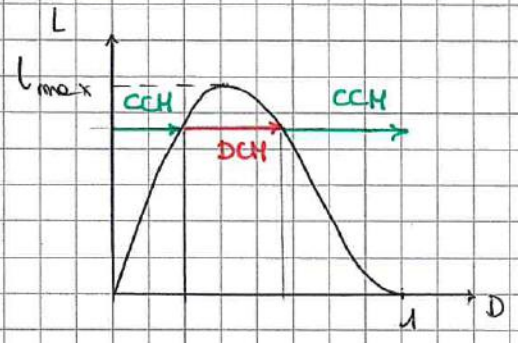
- $\frac{\partial V_o}{\partial D} = G(V_{in}, R, D, \dots) \neq 0$

L, f_{sw} too but they are constant

Comparison CCM - DCM

$$M_{CCM} = \frac{1}{1-D} \qquad M_{DCM} = \frac{1+\sqrt{\frac{2RD^2}{L f_{sw}}+1}}{2} \approx \frac{1}{2} + D\sqrt{\frac{2R}{f_{sw} L}}$$

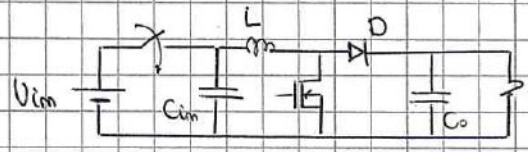
Recall CCM/DCM boundary:



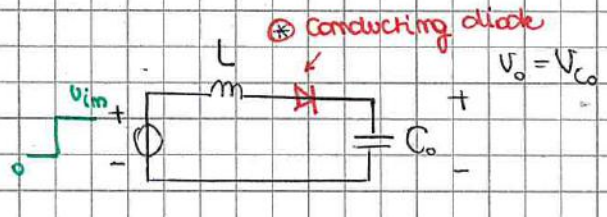
if one chooses an inductor whose value is $L < L_{max}$, what happens is:

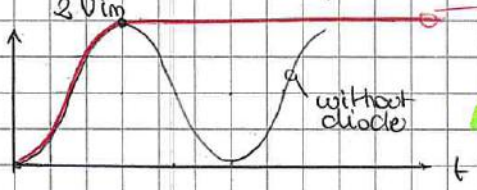
- starting from $D=0$, we are initially in CCM
- as D is increased, we stay in CCM for a while and then step into DCM when we cross the curve
- we stay in DCM as long as we don't cross the curve again, then step back to CCM and stay in CCM until $D=1$

Input voltage step (CIRCUIT TURN ON)



- a large "instantaneous" peak of current affects the inductor because Co must be charged (INRUSH CURRENT)
- a overvoltage reaches the output





START - ON OVERVOLTAGE

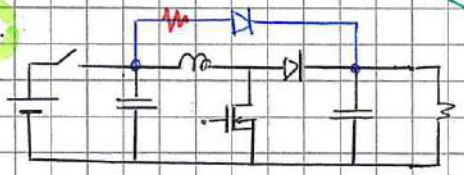
in fact L and Co form a resonant circuit, whose response to a voltage step of amplitude Vim is a voltage of twice that amplitude (2 Vim) initially, that then decreases as the oscillations go on if there are losses (—w—)

2 Vim is the worst case, with no damping resistance

[ideally, in a lossless circuit, oscillations keep 2 Vim amplitude forever]

Possible solutions

a.



So we look for

* the —▷|— sets = Co charge but not discharge, bcs current can't flow back

? Good or bad?
in general bad, unless very low voltages are involved..

- initially, both capacitors are discharged
- when a step is applied to the input (i.e. one switches the converter on) the current flows mainly in —▷|— because $V_o < V_{in}$
  initially 0
- Co is charged quickly to Vim, then Vo increases and becomes $V_o > V_{in}$ So —▷|— gets reverse biased and does not affect the circuit anymore in normal operation
- no voltage drops across L, so it is not resonating

\+ charging initially both Cin and Co to Vim, even if quite aggressively, is a good idea because in normal operation $V_o > V_{in}$, so once the turn on is finished one can start switching S open and closed, increasing D and increasing V_o accordingly

\- this solution is only ok for low powers

\- the inrush current to charge the capacitors may be a problem

- one may add —R— and design its value to get a Q of the RLC resonant circuit of about Q ≈ 0.5

? is it a bad idea from the efficiency standpoint? No because —R— isn't there in normal operation, , because

in old desktops, if one turned it off and then immediately again without letting the NTC cool down enough, the power supply unit wasn't able to get the 2nd time bcs protection wasn't active)

+ in a Boost topology, as a bonus, R_{NTC} is in series to the LC resonant circuit and so, it dumps the oscillations at start-up

NTC:	+ cheap	− failure in power-off and restart
RELAY:	− expensive	+ protection even in " " "

c. this solution works only for Boost, to protect it from output overvoltages: exploit the fact $\sqrt{LC_o} = \tau \gg T_{sw}$ (100 ms) (5 µs)
so we switch before i_L rises up to a large value and starts resonating, i.e. resonance is avoided by INDUCTOR SATURATION (but it is difficult to predict) *

* i.e. when i_L is high $L \to 0$, $\tau \to 0$

Alternative topologies

- Can we move —m— (L) and/or —▷|— (D) from top to bottom?

  a. just one of them: NO! (for EMC reasons!)

  b. both of them: YES, provided that one avoids connecting both V_{in} and V_o to ⏚, otherwise there is a short

  Anyway, there is basically no advantage in moving L and D to the lower side

- Replacing D —▷| with a switch:

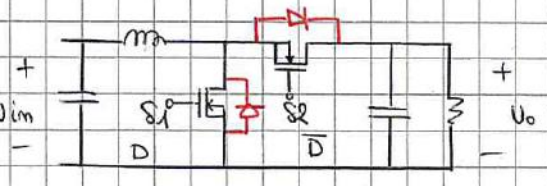
  recall that MOSFETs have a body diode conducting from S to D, so one has to place them in the proper direction!

  Synchronous boost is less common than synchronous Buck because $V_o > V_{in}$, so V_o is likely to be high enough for $V_o \simeq 0.5V - 1V$ not to be a problem

  ↓

  anyway, it has an interesting property:

SYNCHRONOUS BOOST

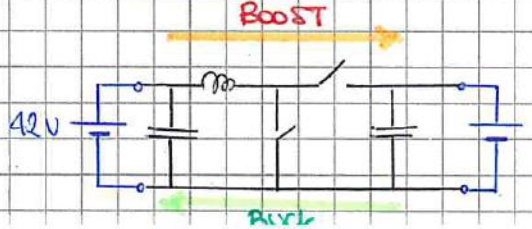


- from left to Right →: synchronous Boost
- from Right to left ←: synchronous Buck

power can be made in both directions!

BIDIRECTIONAL CONVERTER

only works in CCM! (but difficult to control)



#1

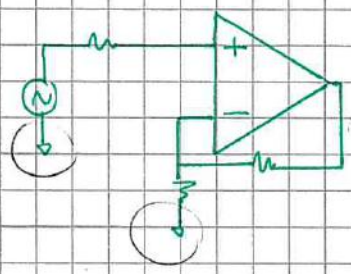
3) potential of the "floor" one is standing on

2) metal box containing electric / electronic circuitry

1) voltage the circuit components / elements refer to

examples:

Signal generator connected to an amplifier



in theory, one can take any voltage as reference

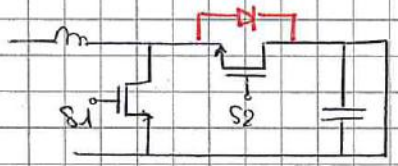
2) has to be connected to 3) for SAFETY REASONS

(to avoid people getting electric shocks if some failure occurs inside the chassis)

1) may / may not be connected to 2)

Beware: if 1) ⏚ is connected to 2) ⏚ (which is not mandatory), it is also connected to 3) ⏚

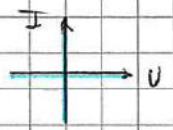
Beware: although it may seem so, synchronous boost CANNOT handle output short-circuits



- one may open S2
- but there is its body diode that will keep conducting

The problem is that switches are not ideal:

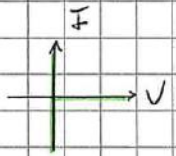
- ideal switch: 4-quadrant operation



(current in both direction can be handled, as well as bipolar voltage)

- MOS transistor: 2-quadrant operation

✓ bidirectional current
× unipolar voltage



(IGBTs as well?)

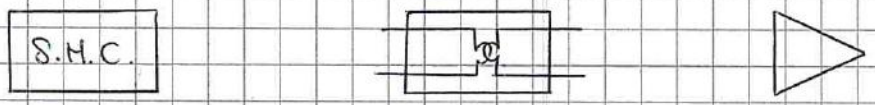
slightly delayed with respect to the other

Another drawback of using S_1 : nMOS is that
S_2 : pMOS
pMOS have worse electrical characteristics !
To have some performances (e.g. carry some current)
$\left(\frac{W}{L}\right)_p > \left(\frac{W}{L}\right)_n$ (by a factor $\simeq 3$) because holes have a lower mobility compared to electrons

And, pMOS have higher $R_{DS,on}$ too !! (for same price) and can stand lower $V_{DS,MAX}$

Switched mode Converter / transformer / amplifier : comparison

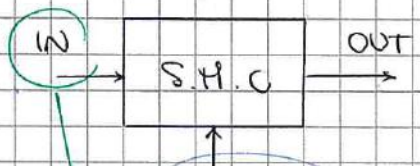
a. b. c.



SM converter transformer amplifier

difference btw a. and b. : a. can convert DC too, b. can't

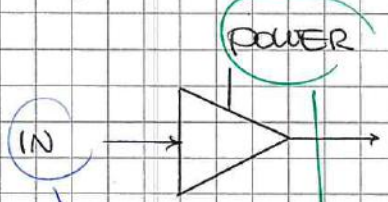
difference btw a. and c. : basically none, just the point of view



input is a power

Control is a signal

If loaded with a speaker and Vin is kept constant, Control signal can be made such as to have at the output an amplified replica : it is an amplifier (class B)



power is not considered an input

the signal is the input

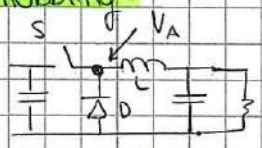
if input signal is constant then output is constant as well : it is a DC voltage supply

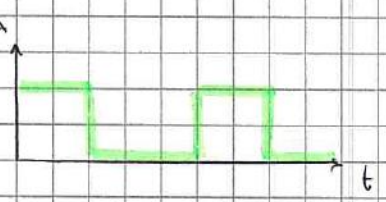
an amplifier is also a converter DC → DC and vice versa

laboratory

OPEN LOOP BUCK

Snubbing





CCM

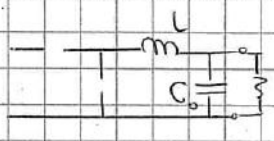
DCM

Observed ringing is bad for EMC. It happens in DCM during T_3 and it is due to parasitic $\neq$ of S and D, which resonate with the inductor L. During T_3:

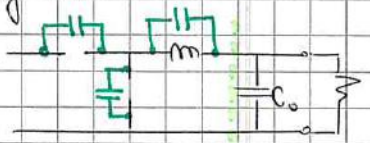
ideal and observed

ideal

observed



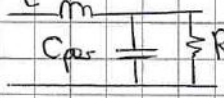
ideally



actually

where C_{par} is the Σ of all parasitic $\neq$ which are in $\parallel$ but its value is unknown!

To damp a resonant circuit a resistance is needed:



the Q of such a circuit is

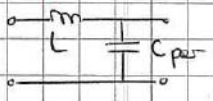
$$Q = \frac{R}{Z_0} \quad \text{where} \quad R = R_{snub} \text{ (parallel res.)}$$

Z_0 : characteristic impedance $\quad Z_0 = \sqrt{\frac{L}{C_{par}}}$

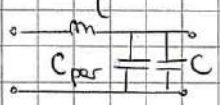
We impose $Q = 0.7 \div 1$ to damp the ringing reasonably but to do that we need to know Z_0 and therefore C_{par} (in principle we know the nominal $L = 220\,\mu H$, but if we measure it too it is even better)

- we observe V_A on the scope and measure the resonance freq. of the ringing we call it f_{res} and we know it is:

$$f_{res} = \frac{1}{2\pi\sqrt{L \cdot C_{par}}}$$



- we add a small capacitance of known value (e.g. 1 nF) in parallel to C_{par} (on the real circuit, either in $\parallel$ to S or to D)



we measure the new ringing frequency, which will be different (smaller), and we know its expression is

$$f'_{res} = \frac{1}{2\pi\sqrt{L(C_{par} + C)}}$$

where C_{par} is still unknown but C is known bcs it is an external component we chose

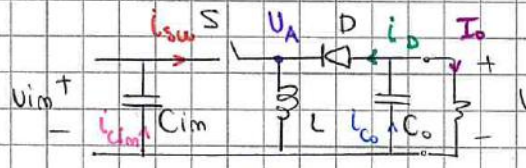
- we take the ratio

$$\frac{f_{res}}{f'_{res}} = \sqrt{\frac{C_{par} + C}{C_{par}}} \quad \Rightarrow \quad C_{par} = \frac{C}{-1 + \left(\frac{f_{res}}{f'_{res}}\right)^2}$$

BUCK - BOOST

24/10/2014

- it was called fly-back in the past; nowadays fly-back is a different topology
- it may be called UP-DOWN converter, because $\frac{V_o}{V_{im}} < 0$ (or even "inverting")

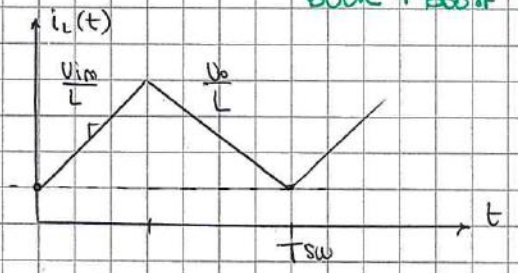


- not used so much as it is, but its derivative is the most widely used because it's the cheapest
- the sign convention for V_o and I_o is the same used for the other topologies, because in principle we don't know yet that V_o has opposite sign wrt V_{im} (negative signs will pop up in the analysis)

this is not enough to conclude that the Buck-Boost is Buck + Boost

- input: switch in series, like Buck
- output: diode in series to output section (Co // load), like Boost

CCM

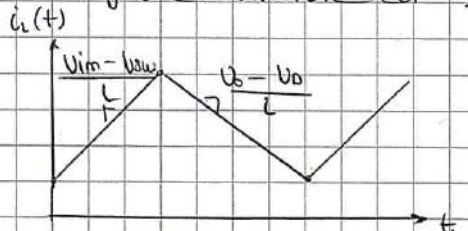


- used 4 assumptions
- usual way of finding M from Δi_L during T_{on} = Δi_L during T_{off}

$$\frac{V_{im}}{L} T_{on} + \frac{V_o}{L} T_{off} = 0 \quad \rightarrow \quad \frac{V_o}{V_{im}} = M = -\frac{T_{on}}{T_{off}} = \frac{D}{D-1}$$

Notice: like in all CCM converters we analyzed, M does not depend on L, f_{sw}, load, ... but just on D

If we considered losses:



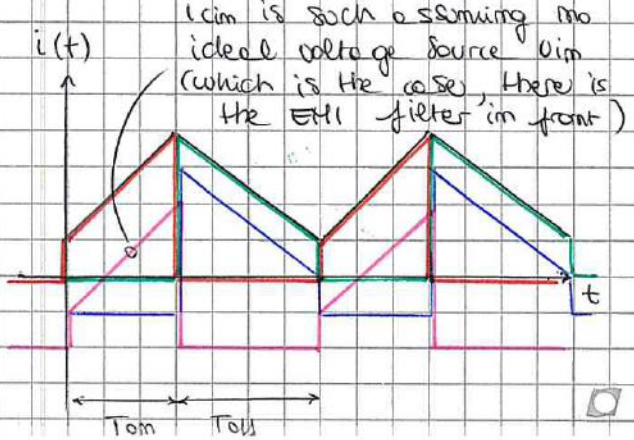
D_{real} to get the same V_o, given the same V_{im}, is larger than D_{ideal} computed assuming no losses

or, equivalently, with a given D the V_o one actually gets is lower than what expected from lossless analysis

Waveforms

- $i_{sw} = \begin{cases} i_L & T_{on} \\ 0 & T_{off} \end{cases}$
- $i_D = \begin{cases} 0 & T_{on} \\ i_L & T_{off} \end{cases}$
- $i_{Cim} = i_{sw} - \overline{i_{sw}}$
- $i_{Co} = i_D - \overline{i_o}$

both C_{im} and C_o are heavily stressed



i_{sw}, i_D are the same as for Buck and Boost, whereas i_{Cim} and i_{Co} change from topology to topology

For eq. 8 we need to relate I_o to some current flowing in the circuit

$$I_o = \frac{v_o}{R} = \left(-\overline{i_D}\right) = -\frac{I_{MAX} + I_{min}}{2}(1-D) \qquad \text{eq. 8}$$

because of the sign convention we chose for i_D and I_o

$$\begin{cases} I_{MAX} - I_{min} = -\dfrac{v_o}{f_{sw}L}(1-D) \\ I_{MAX} + I_{min} = -\dfrac{2v_o}{R(1-D)} \end{cases}$$

$$I_{MAX} = -\frac{v_o}{(1-D)R} - \frac{v_o(1-D)}{2f_{sw}L}$$

$$I_{min} = -\frac{v_o}{(1-D)R} + \frac{v_o(1-D)}{2f_{sw}L}$$

We use them for: CCM/DCM boundary (I_{min}); current stresses (I_{MAX})

CCM – DCM boundary

$$I_{min} = 0 \iff -\frac{v_o}{(1-D)R} + \frac{v_o(1-D)}{2f_{sw}L} = 0$$

$\Updownarrow$

R: design constraint
D: " "
f_{sw}: free parameters (chosen first)
L: " " (derived)

$$L_c = \frac{R(1-D)^2}{2f_{sw}}$$

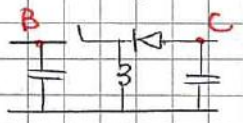
Good news: $(1-D)^2$ is monotonic → easier to study than Boost 🙂

CCM: $L > L_c = \dfrac{R_{MAX}(1-D_{min})^2}{2f_{sw}}$ lightest load

DCM: $L < L_c = \dfrac{R_{min}(1-D_{MAX})^2}{2f_{sw}}$ heaviest load

Stresses: capacitors

Since both are under heavy stress, one can use quadratic KCL at nodes B and C without numerical cancellation to occur



Input / output protection

✓ protection from output short circuits

(just open S and source is protected)

✗ no immunity from input overvoltages

(if S is closed the overvoltage can damage D, because L does not change it so much if the overvoltage has a very short duration & it does not "absorb" it; if S is open, S itself can be damaged)

✓ load can be switched off

(i.e. disconnected from the source just by opening S)

2) DISCHARGE PHASE

$P_o = R I_o^2 = \frac{V_o^2}{R}$ (power dissipated by the load), $P_o = P_{in}$ if there are no losses

By equating the expressions:

$$\frac{V_o^2}{R} = \frac{V_{im}^2 D^2}{2 L f_{sw}} \Rightarrow M = \frac{V_o}{V_{im}} = \pm D \sqrt{\frac{R}{2 L f_{sw}}}$$

meaningless

Notice: input-output relation (i.e. conversion ratio M) is linear in D, meaning that the gain is constant in D

- M depends on R, because we are in DCM
- $R \to \infty$ (disconnected load): $M \to \infty \iff V_o \to \infty$ if $D = const.$ So ka-boom, don't try this at home / in lab (one has to design the controller in such a way that $D \to 0$ if $R \to \infty$, so V_o stays under control)

Converter parameters for a DCM Buck-Boost

- $\frac{\partial V_o}{\partial V_{im}} = M$ (as usual)
- $\frac{\partial V_o}{\partial D} = -V_{im} \sqrt{\frac{R}{2 L f_{sw}}}$

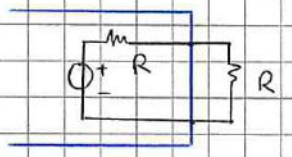
28/10/2014

- $\frac{\partial V_o}{\partial I_o} \neq 0$ (as it happens in any DCM converter)

$$\frac{\partial V_o}{\partial I_o} = \frac{\partial}{\partial I_o}\left(\frac{V_{im}^2 D^2}{2 f_{sw} L I_o}\right) = -\frac{V_{im}^2 D^2}{2 f_{sw} L I_o^2} = -\frac{V_{im}^2 D^2 R^2}{2 f_{sw} L V_o^2} = -\frac{D^2 R^2}{2 f_{sw} L} \cdot \frac{1}{M^2} =$$

$$= -\frac{D^2 R^2}{2 f_{sw} L} \cdot \frac{2 f_{sw} L}{D^2 R} = -R$$

output resistance is equal (in magnitude) to the load resistance



Buck-Boost

From this circuit, it looks like that $\eta_{max} = 50\%$

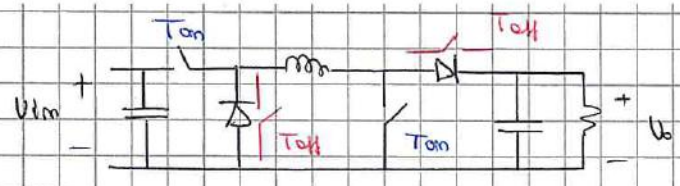
BUT

Our circuit is (ideally) lossless, has no dissipative elements, so the efficiency is supposed to be $\eta = 100\%$.

In fact, it is!

Beware: one must distinguish between DIFFERENTIAL RESISTANCE and POWER RESISTANCE

↳ output internal resistance is not a true resistor, whose VI relation is linear (and for which differential and power resistance always coincide): the VI curve is non linear and so $\eta = 100\%$. Despite the differential



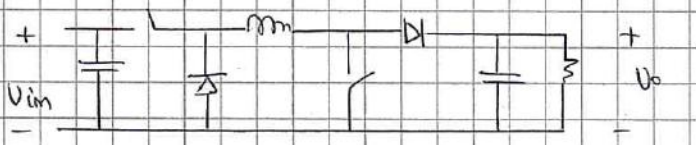
NON INVERTING BUCK - BOOST

cascade of a buck (non-inverting) and a boost (non-inverting)

$\frac{V_o}{V_{im}} > 0$

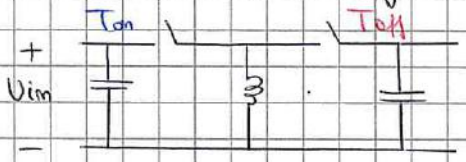
- seems expensive because it has 2 switches and 2 diodes (for low-voltage appl. we want to replace diodes with switches —|— that have a lower ON voltage drop, to improve η) → in which case 2 are low-side and 2 are high side but 1 inductor only !!
- has the advantage of giving V_{im}, V_o with same sign and any magnitude relation between them (may be used to get a DC voltage from a battery, whose voltage V_{im} is > V_o when fose and < V_o when down)
- Still an INDIRECT Converter !

How to get to the "standard" topology we are used to:

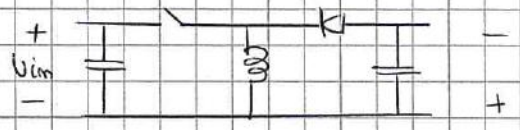


—m— is connected btw Vim and gnd during Ton and btw Vo and gnd during Toff:
one of its nodes is always to gnd, but it is not the same node in both phases

⇒ one can force one terminal of the —m— to be always grounded: the only difference is that now the —m— is no longer turned upside down when going from Ton to Toff and vice versa



- swapping the ends of the inductor causes no difference in the charge / discharge: it just reverses the output voltage sign!
- If instead of 2 switches we use a switch and a diode the diode must be reversed to allow current flow during Toff:



we get to the BUCK - BOOST that we used to know

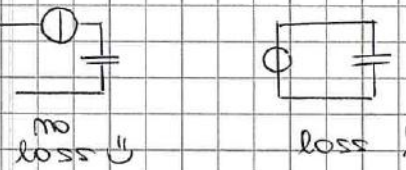
$\frac{V_o}{V_{im}} < 0$

charge and discharge !

⇒ energy transfer is LCL, no power loss

(connecting C to L causes no energy loss, because it is like connecting a voltage source ⊕ to a current source ⊖ and vice versa)

↑ —m— look like -⊡-

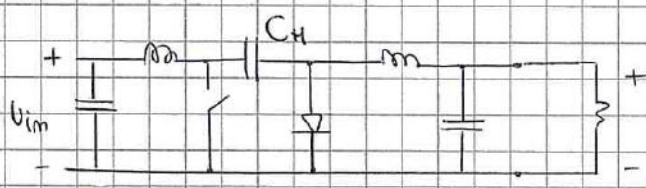


Notice: the Boost-Buck is an INDIRECT CONVERTER as well, because C_H first charges because connected to the input (T_{off}) and then discharges because connected to the output (T_{on}): it is never connected to input and output at the same time !

Let us do the opposite as we did in the Buck-Boost ↘

Instead of keeping one end of the ⊣⊢ cap. grounded all the time, we can flip it over any time we go from T_{on} to T_{off} and vice versa

i.e. make the capacitor "floating", connecting a —|— to one of its side and a ⊣⊢ to the other's side, so that in each phase one of its terminals is grounded



$$V_o = -\frac{D}{1-D} V_{in}$$

✓ we can get rid of 2 switches (1 switch and a diode)

It works exactly as before, except for the fact that C_H is flipped over every time from T_{on} to T_{off}

⇒ just a sign change in V_o !

⇒ the conversion ratio is now exactly as the one of the Buck-Boost

− Main disadvantages: − can be controlled in DCM only
− heavy and expensive due to 2 inductors

↳ good news about this: one can find the way of winding both coils on the same magnetic core !! integrated magnetics

↳ bad news about the good news: it is very difficult to do it !!

+ Main advantage: input and output currents are both smooth (in CCM !)

very limited stress !

Notice: C_H can be electrolytic, it undergoes no polarity inversion (voltage)

For the Boost soft start is not possible because if $D \to 0$ the input voltage is applied to ⊸ for a long time, which makes it saturate eventually

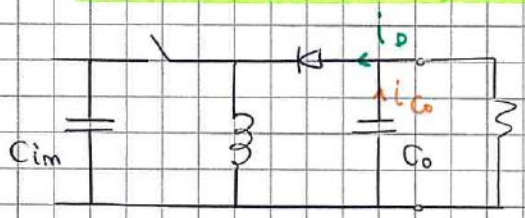
meaning, it becomes as a piece of wire, which makes its magnetic properties "disappear"

Surprise:

there are more basic topologies, (which come out from different combinations of ⊸, ⊣, ⊸ ?) but they won't be analyzed in this course

ABOUT INPUT / OUTPUT CAPACITORS

In a Buck - Boost (DCM)



C_{in}: has to prevent EM noise from entering the source

C_o: is the energy source for the load during Toff

Choice of C_o

relevant parameters:
- working voltage
- RMS current

} for stresses

- ESR / C_o : to control output voltage ripple

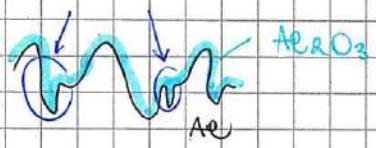
↑ electrolytic cap. ↑ film / ceramic cap.

$i_{C_o} = i_D - \overline{i_D} = i_D - I_o$

for i_{C_o} to have no DC comp., areas and have to be equal

the dielectric should have constant thickness and must cover the rough surface precisely, without filling holes: it cannot be deposited, Al_2O_3 is grown oxidizing Al of the surface itself

- the thickness of dielectric we grow is limited by below by the voltage we want the it to withstand (the BREAKDOWN voltage)
- if we grow a too thick oxide we lose area, because narrow valleys are filled up



Advantages

1. Dielectric constant is high enough: $\varepsilon_{r\,Al_2O_3} \approx 11$
2. Al_2O_3 can withstand quite a high voltage without breaking down

- then we need to grow the second metal plate on top
But we have a problem: how to grow a plate whose rough surface mirrors that of the first plate exactly?
  - surely we can't by etching
  - we could with a liquid, that can follow the shape of the surface

    ⇓

    we use "water" (ELECTROLYTHIC SOLUTION)

    which follows the shape of the first layer exactly

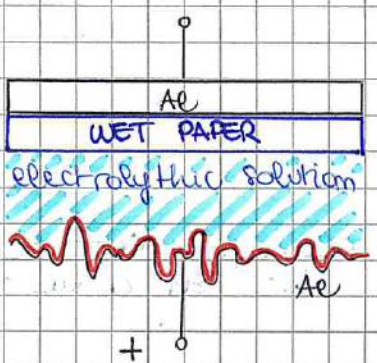
    and then a "tank" is needed for water not to evaporate:

- a layer of wet paper is placed on top which is the source that resupplies electrolytes to the solution when they evaporate
- a layer of Al foil is contacted to the paper and forms the outer plate of the capacitor

? Why do electrolytic caps have a + and a − ? What happens if polarity is reversed?

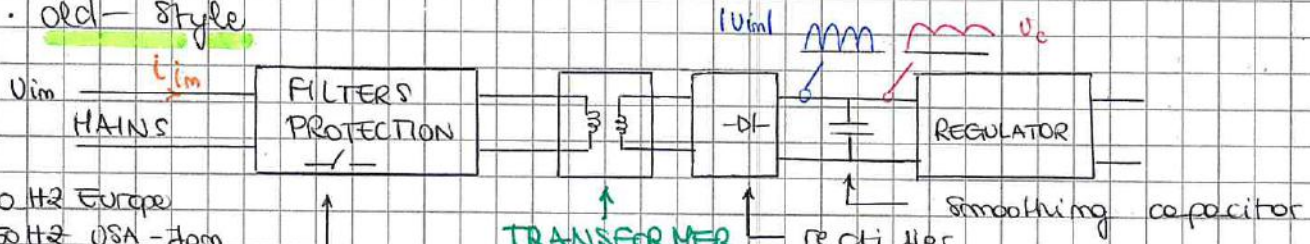
They explode. Why?

Ions that make up Al_2O_3 are Al^{+}_{2} and O^{-}_{3} and O^{-}_{3} ions in water must be forced to stay close to the Al plate which needs therefore to have a positive side



RECTIFIERS

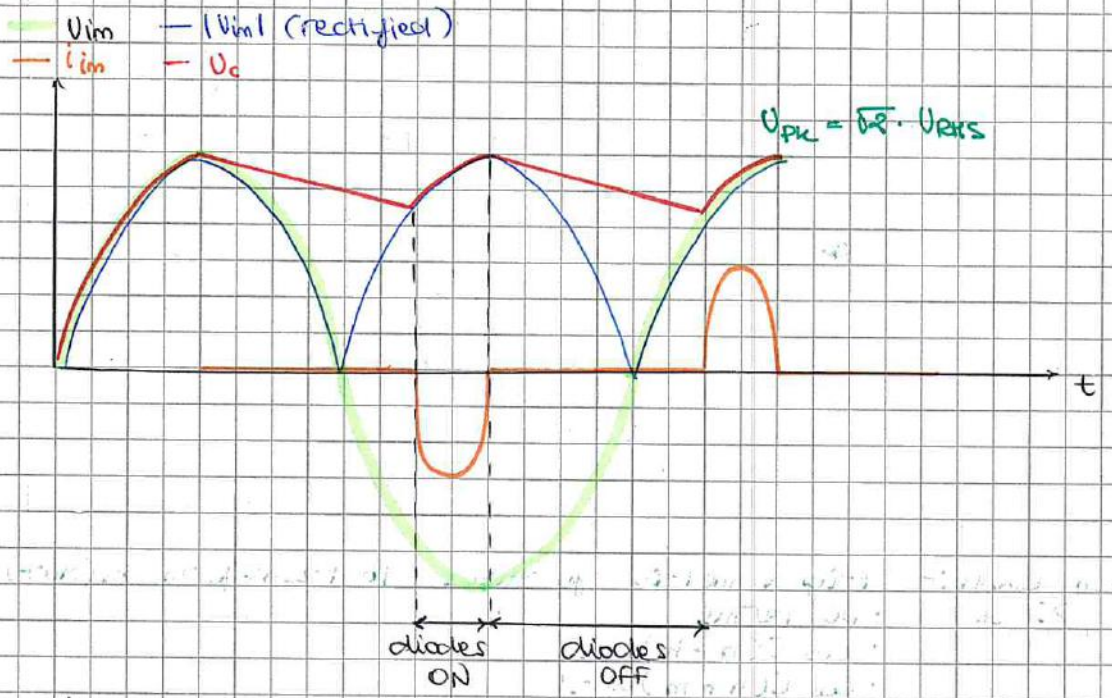
- AC → DC conversion, typically from mains
- old-style



50 Hz Europe
60 Hz USA - Japan
400 Hz airplanes

needed for
- noise
- over voltages

needed to:
1) provide galvanic isolation
2) step-down in voltage (from 230 V (RMS) to lower voltage!)



Main disadvantages:

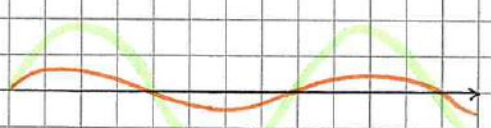
1) 50 Hz transformer: heavy and costly
2) current iim absorbed from mains is impulsive

because diodes conduct just for the short time needed to recharge the capacitor after each half-cycle

⇒ the old-style rectifier is a non-linear load to the main, because Vim and iim are not proportionale, because of diodes!

International EMC rules forbid to absorb impulsive current from mains! the converter must look like a resistor

i.e. absorb a sinusoidal current (if the input voltage is sinusoidal!) in phase with the voltage

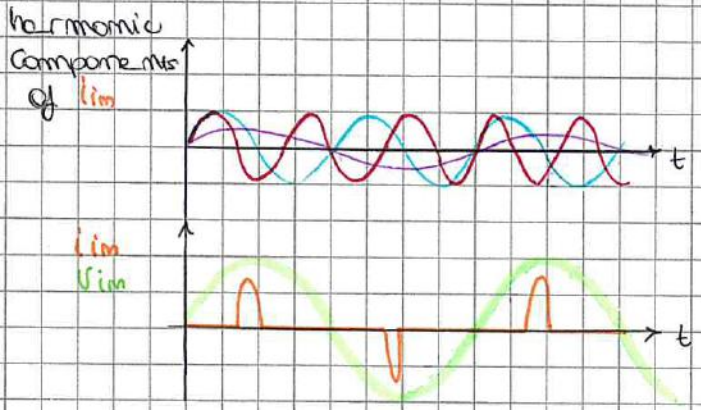


The reason goes as follows:

$$= \frac{V_{PK} \cdot I_{1PK}}{2} \cos(\varphi_1) = \overline{P}$$

power the user uses and pays for

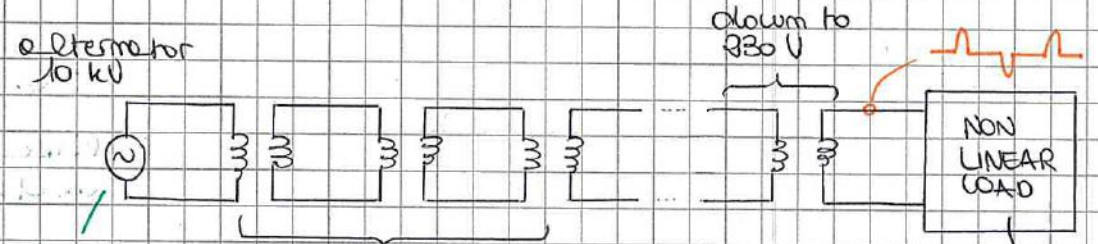
1st harmonic of input current carries some power (active!)
2nd " " " " does not carry any power (active!)
3rd " " " " " " " (active!)



— fundamental
— 2nd harmonic
— 3rd harmonic

φ_1: displacement (phase shift) between v_{in} and the fundamental component of i_{in}

On the other hand, what causes power losses (e.g. on the wires) is not average power but APPARENT POWER, to which all harmonics contribute!



power used by non-linear load: $\overline{P} = \frac{V_{PK} I_{1PK}}{2} \cdot \cos\varphi_1$

power dissipated in the wires: $P_{loss} = R_{wire} \cdot I^2_{RMS}$

The whole power distribution system (wires, transformers, ...) is loaded with (overloaded, actually)

$P_{app} = V_{RMS} \cdot I_{RMS}$ APPARENT POWER

but what users pay for is just

P_{active} (real) (average) $= V_{RMS} \cdot I_{1RMS} \cdot \cos\varphi_1$ ACTIVE POWER

($\frac{1}{2}$ has been split into $\frac{1}{\sqrt{2}}$ and $\frac{1}{\sqrt{2}}$ and included in the RMS)

I_{RMS}: all the harmonics contribute

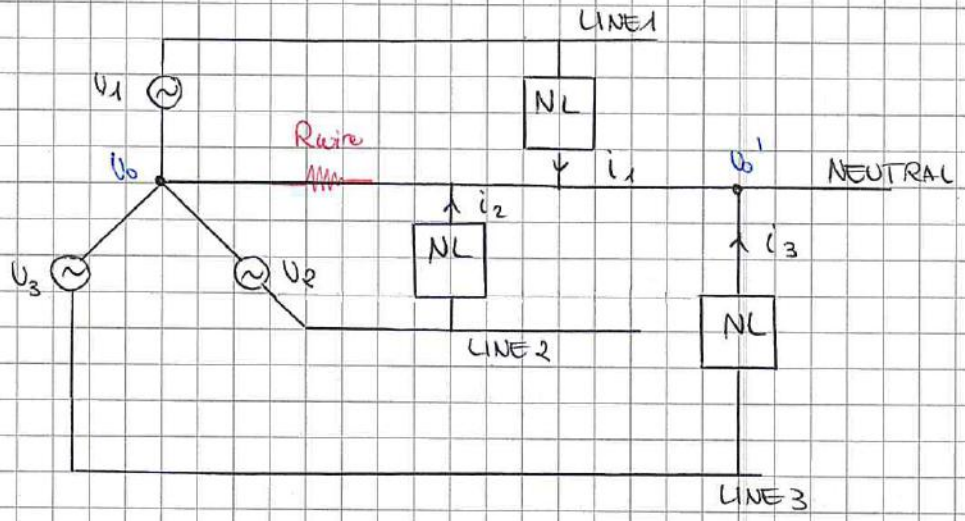
I_{1RMS}: only the fundamental contributes

This was true in the past, when loads were linear:

- lamps / bulbs (—ω—)
- motors (—ω— + —ωm—)

Nowadays, most of loads are non-linear !!

- tv sets
- white goods
- all the electronics!

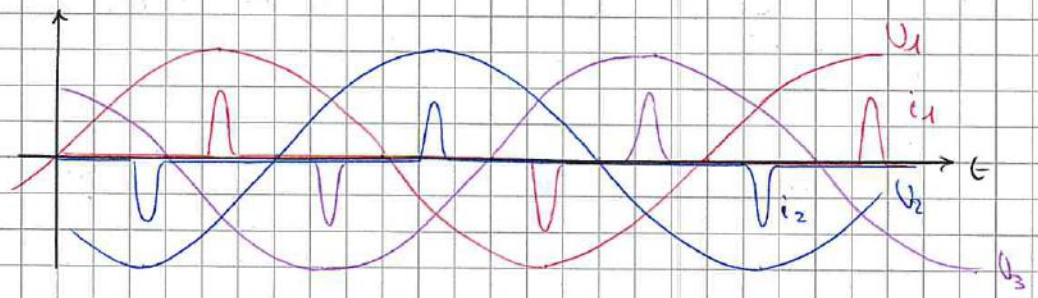


b.

non linear loads

The 3 voltages keep being out of phase by 120°, and this is no problem in itself.

The problem is that now i_1, i_2, i_3 are impulsive and out of phase, no cancellation occurs in $i_{NEUTRAL}$!



⇒ $i_{NEUTRAL}$ is pulsating and large

and if the NEUTRAL wire is still small as before its resistance causes a significant voltage drop $R_{wire} I^2_{NEUT,RMS}$ which makes $v_0' \neq v_0$

⇒ there is a current noise that disturbs all loads connected to the distribution system

The reason for the current being pulsating is putting together $\rightarrow\!|$ and $\frac{1}{T}$ $\Rightarrow$ nowadays one can't even sell such systems bcs we know in advance they won't be compliant with international rules $\Rightarrow$ we have to get rid of either one

1) get rid of $\frac{1}{T}$

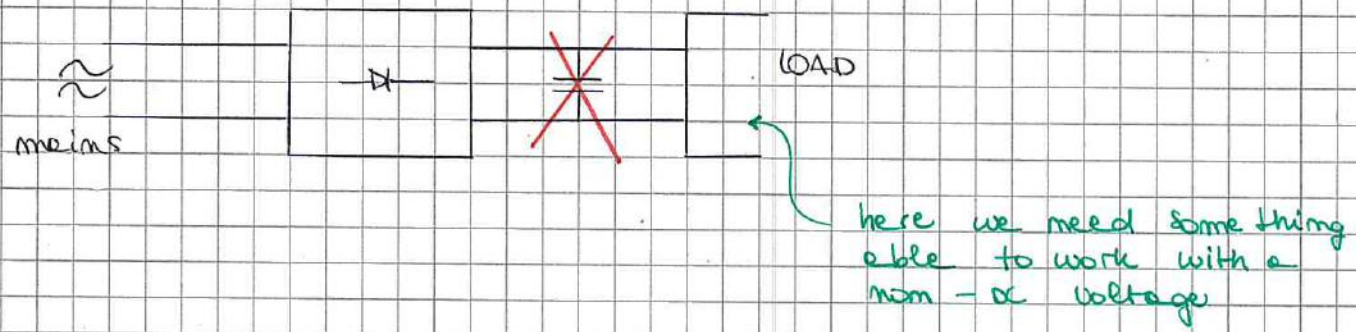
2) get rid of $\rightarrow\!|$

Possibilities:

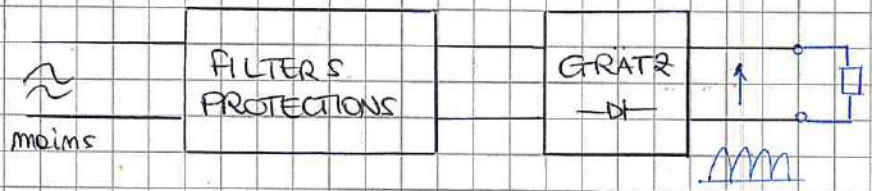
2) ABSOLUTELY NOT !

we can't supply the load with a voltage that changes sign because we damage it!
If we can't have a "true" DC output voltage, we need at least
- a constant sign voltage, having
- a non-zero DC component

1) CAN BE DONE



- modern power supplies look like



\+ no 50 Hz transformer

\- output voltage is not DC (although it has non-zero DC comp.)

\- " " has a very high peak ($\sim$ 325 V)

\- no isolation

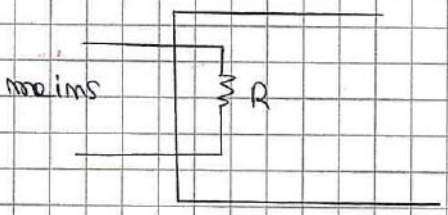
\+ no impulsive current absorption if a load is inserted

This is not the final structure !

31/10/2014

PFC

- the converter must look as a resistor (linear load) to the mains: it must sink an undistorted sinusoidal current and a voltage in phase with the current
- in fact, if nothing is done to correct for it, the converter sinks a distorted pulsating current, with high harmonic content => this causes AP >> RP

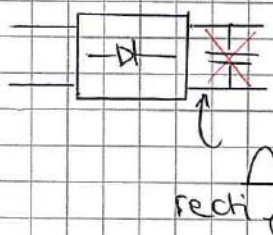


apparent power: $U_{RMS} \cdot I_{RMS}$ (all harmonics)

active (real) power: $U_{RMS} \cdot I_{1\,RMS} \cdot \cos\varphi_1$ (only fundamental)

the cause of this non linearity is the cascade → + ⏚

- AP is what the energy provider must pay for (in terms of transmission lines and transformers)
- RP is what the customer pays for
- if load is linear: AP = RP → ENEL is ☺
- if load is non linear: AP > RP → ENEL is ☹
- power factor: $PF = \frac{I_{1\,RMS}}{I_{RMS}} \cdot \cos\varphi_1$ — $\cos\varphi_1$: displacement factor; $\frac{I_{1\,RMS}}{I_{RMS}}$: distortion factor



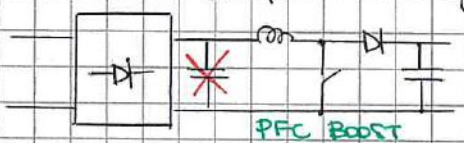
for the load to be linear, we have to get rid of the cascade of rectifier and capacitor

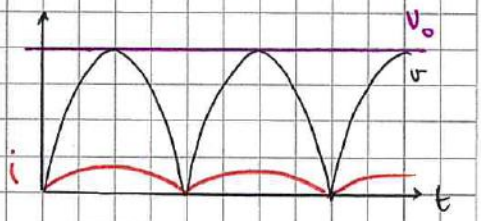
- can't get rid of rectifier

⇒ - must get rid of capacitor

but a DC → DC converter cannot handle the rectified sinusoidal as it is, because it is not a DC voltage at all, although it has a non-zero DC component

we need a high-efficiency circuit, a switched-mode converter in fact, that is able to take $v_{\sim}$ and convert it into a constant output voltage V_o ——



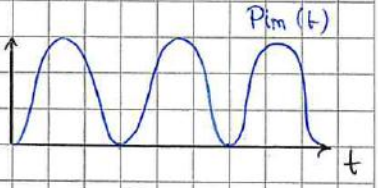


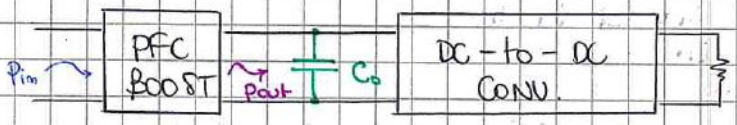
a. we have already seen that BUCK is not a good choice

b. we must drive the Boost in such a way to force it to sink exactly the —— current, if we choose properly V_o (i.e. in such a way that it is ≥ than the peak of $v_{\sim}$)

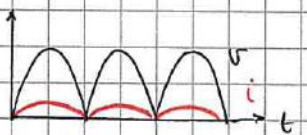
Power mismatch

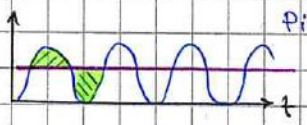
- instantaneous input power $P_{in}(t)$ the PFC absorbs is NOT constant (it is given by the product $v \times i$ and it is a (sinusoid)^2 wave form) because it has to look like a resistor
- output power it has to provide to the following stage, which is in turn a DC to DC converter, is constant because its input voltage is constant $\Rightarrow$ there is a POWER MISMATCH





P_{in} : not constant
P_{out} : constant (if load constant)
if $\eta = 100\%$: $P_{out} = \overline{P_{in}}$





$P_{in} = v \times i$
$P_{out} = \overline{P_{in}}$

Storage of electric energy: $\dashv\vdash$ or $\frac{1}{3}$

PFC BOOST is forced to sink a non constant input power to look like a resistor but it has to source a constant output power bcs the following block is a DC - to - DC converter

we place a $\dashv\vdash$ in btw PFC and following converter as a BUFFER
($\dashv\vdash$ are smaller (lighter) less expensive than $\frac{1}{3}$ for the same amount of stored energy)

for some part of the cycle $P_{in} > P_o$
for the remaining part of the cycle $P_{in} < P_o$
the two areas ▲ and ▼ equal $\Rightarrow$ need an <u>energy storage</u>

output capacitor C_o of the boost does the job, but this implies that the voltage across it is not constant, it changes as energy is stored (released)

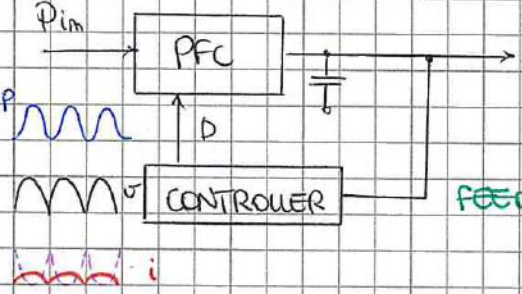
$\Rightarrow$ V_o of the boost, which is V_{in} for the following DC → DC converter, has a voltage ripple whose frequency is $2 \times f_{mains}$ (e.g. 100Hz)

We need to determine the value of C_o $\dashv\vdash$ because it works at freq. $2 \times f_{mains}$ which is low enough for any capacitor to really look like a capacitor!

C_o is determined based on energy considerations

PFC CONTROL

Once we selected the proper topology and clarified what kind of waveforms we need to obtain (sinusoidal input current, in phase with input voltage, approximately constant output voltage): we need to design the controller!



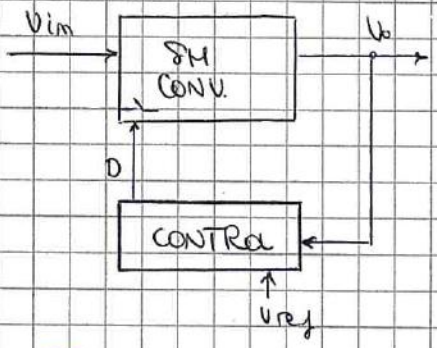
- the PFC cannot be work as such without some output voltage ripple
- if one designs the controller to get V_o = constant exactly (i.e. $\Delta V_o = 0$) it means that the capacitor C_o is neither charged nor discharged
  - ↳ trying to absorb input power constant, while v_{in} being a (rectified) sinusoid, implies forcing input current to be ⩘⩘⩘ rather than ∩∩∩
- ΔV_o must be there, otherwise the PFC is not a PFC!
- the controller must sense and control $\overline{V_o}$ only, but not V_o! The average value must be kept to the specified value but the ripple MUST NOT be eliminated

  ↳ we need a LOW-PASS FILTER with a cutoff frequency well below the ripple frequency $2 \times f_{LINE}$

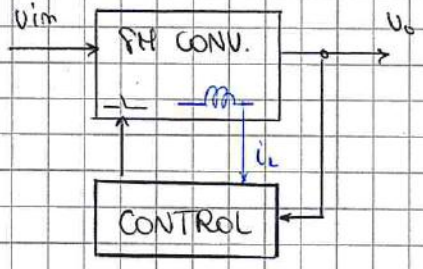
(the controller is itself a filter!)

The bandwidth of the controller being very limited ($BW \ll 2 \times f_{LINE}$, ≃ 10 Hz) is what enables us to control a Boost in CCM despite the RHP zero!

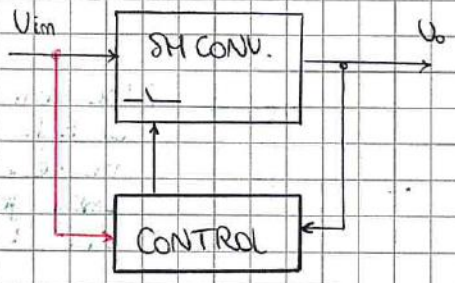
CONTROL OF SWITCH MODE CONVERTERS



a. FEEDBACK CONTROLLER VOLTAGE MODE



b. FEEDBACK CONTROLLER CURRENT MODE



c. VOLTAGE FEED-FORWARD CONTROLLER

The most immediate way one can think of to keep V_o constant (almost, apart from the ripple) is to sense it (measure it), compare it to a reference and adjust the duty cycle to keep it to the level it is supposed to be:
this is a voltage mode

But there are other ways:

modern control theory is based on the sensing of all of the state variables of the system
- V_o is a state variable bcs it is the voltage across capacitor C_o and it must be sensed in any case!
- the other state variable of a SM converter is the current through the inductor

b. Current Mode controllers sense <u>both</u> output voltage and inductor current

VM and CM will be analyzed in this course.

Another way may be:

sensing V_{in} to be able to correct for its change before all state variables have been modified

This is quite an old technique and it is called
c. Voltage feed forward

Hystorically, voltage mode was invented first, then voltage feed forward came and, at last, current mode was invented "by mistake": CM includes voltage feedforward in itself, so voltage feed forward alone dropped out of use.

Plant modelling basic steps

Start from
- Non Linear
- Time Varying

circuit (our SH Converter)

we do it in 2 steps

must get to
- Linear
- Time Invariant

circuit to be able to apply all the techniques.

AVERAGING: there are multiple ways of doing it, corresp. to different approx. leading to approximately the same result

LINEARIZATION: there is a unique technique to do it

One of these averaging techniques is:

a. $\overline{x(t)} = \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} x(\tau)\, d\tau$ MOVING AVERAGE

(a window one-period-long moves along the waveform)

$\overline{x(t)}$ is a continuous function of time, because the average is computed at any instant while the window is shifting

when averaging, info on the waveform is lost!

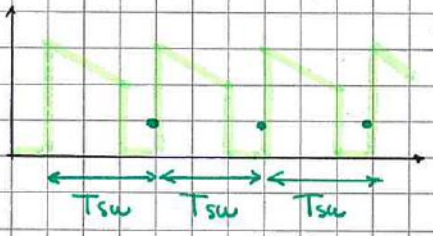
4/11/2014

Recall: 2-step modelling of a SH converter / averaging \ linearization

Other averaging techniques:

b. each cycle is "compressed" into a single value (its average): a discrete set of numbers is got instead of a continuous fn.

$$x(nT_{sw}) = \frac{1}{T_{sw}} \int_{(n-1)T_{sw}}^{nT_{sw}} x(\tau)\, d\tau$$

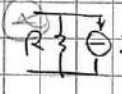


$x(nT_{sw})$ is a sequence of numbers, as many as the n° of cycles one averages over.

Recall: basic mathematical tool to deal with time-discrete systems is Z-TRANSFORM (provided that they are linear, or once they have been linearized)

In this case (resistive load) the only forcing input is V_{in}

Be aware: if we had a generic non linear load described by its Norton equivalent circuit (parallel of resistor and current sink) we would have to include I_0 among the inputs, because it is a forcing term - known - not something we want to find out!



a. $$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in}$$ during T_{on}

$$\dot{x} = A_1 \cdot x + B_1 \cdot u$$

b. $$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in}$$ during T_{off}

$$\dot{x} = A_2 \cdot x + B_2 \cdot u$$

In principle there is a way of getting the solution by solving these systems directly:

- Solve system a., evaluate the solution for $t = T_{on}$ and use these final conditions as initial conditions for system b.
- Solve system b. using the initial condition computed in the previous step, evaluate the solution for $t = T_{sw}$ and use these final conditions as initial conditions for system a.
- keep going like this as long as needed

This is a very time consuming method but one gets the full waveforms, with all information in it.
It can be done by Matlab, but it is computationally heavy.

But then, prof. Middlebrook got an idea:

Sum the 2 equation together giving to each the proper weight (D and $(1-D)$), i.e. compute a weighted average

$\dot{x} = A_1 x + B_1 u$ weight: D
$\dot{x} = A_2 x + B_2 u$ weight: $1-D$

STATE SPACE AVERAGING

$$\dot{x} = (A_1 D + A_2 (1-D)) x + (B_1 D + B_2 (1-D)) u$$
$$= \dot{x} \cdot D + \dot{x}(1-D)$$

Notice: taking an average, in general, implies a loss of INFORMATION

- waveform IS lost (peak, rms values, ..)
- average values are retained