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A P P U N T I

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Master Degree in Electronics

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"Best Notes"
A.A. 2013-2014

NOTE: INSTEAD OF PROVIDING EXERCISES DONE IN CLASS (NUMBERS AND SOLUTIONS ARE AVAILABLE ON THE WEB), I'VE SUMMARIZED THE BASIC CONCEPTS AND FORMULAE WHICH ARE USEFUL TO SOLVE EXERCISES IN SOME "EXAMPLES"

MOS AND BIPOLAR TRANSISTOR

FOR BOTH OF THEM:

- STRUCTURE
- BEHAVIOUR
- INPUT CHARACTERISTIC
- OUTPUT CHARACTERISTIC
- EQUATIONS
- SMALL SIGNAL MODEL
- LARGE SIGNAL MODEL
- PARASITIC CAPACITANCE
- DIFFERENCES

BJT

A BIPOLAR JUNCTION TRANSISTOR IS A TYPE OF TRANSISTOR THAT RELIES ON THE CONTACT OF TWO TYPES OF SEMICONDUCTOR FOR ITS OPERATION. IT'S SO NAMED BECAUSE ITS OPERATION INVOLVES BOTH ELECTRONS (N REGIONS) AND HOLES (P REGIONS); THESE TWO KIND OF CHARGE CARRIERS ARE CHARACTERISTIC OF THE TWO KINDS OF DOPED SEMICONDUCTOR MATERIAL. CHARGE FLOW, IN A BJT, IS SO DUE TO BIDIRECTIONAL DIFFUSION OF CHARGE ACROSS A JUNCTION BETWEEN TWO REGIONS OF DIFFERENT CHARGE CONCENTRATIONS.

EVERY REGION IS EQUIPPED WITH A TERMINAL, SO THERE ARE 3 TERMINALS:

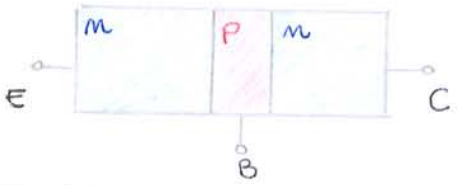

FIG A1.4 : "old" representation for a N-P-N BJT

FIG A1.5 "modern" representation for a N-P-N BJT

1. EMITTER → N REGION, DOPING OF THE ORDER OF $\sim 10^{20}$
2. BASE → P REGION, DOPING OF THE ORDER OF $\sim 10^{17}$
3. COLLECTOR → N REGION, DOPING OF THE ORDER OF $\sim 10^{15}$

SO, SINCE THE ORDER OF THE DOPING IS DIFFERENT, THE BJT IS NOT A SYMMETRIC DEVICE!

WE'VE CONSIDERED A N-P-N DEVICE BUT WE CAN ALSO CONSIDER A P-N-P DEVICE.

THEIR SYMBOLS ARE:

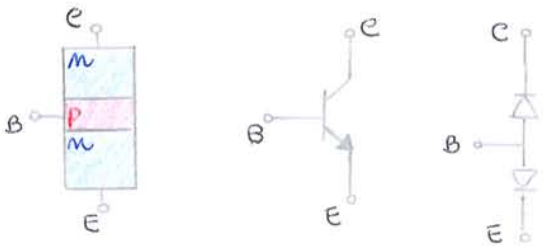

FIG A1.6 N-P-N BJT symbols

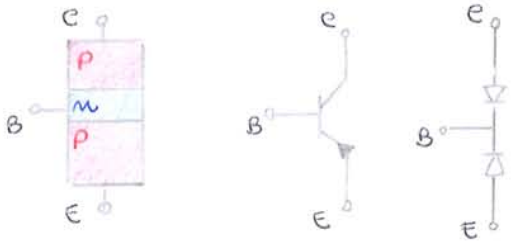

FIG A1.7 P-N-P BJT symbol

THE BJT IS A CURRENT CONTROLLED DEVICE: WE CAN CONTROL THE C-E CURRENT BY THE B-E CURRENT; IT'S A NOURISHMENT CURRENT, SO WHEN $I_B = 0$ THERE'S NO C-E CURRENT NEITHER.

THAT'S WHY USUALLY WE FIND A RESISTANCE ON THE B TERMINAL: IT ALLOWS TO REGULATE THE CURRENT FLOW AND PREVENTS THE APPLICATION OF HIGH INPUT SIGNALS.

IN FIG. A1.8 THE BJT INPUT CHARACTERISTIC IS SHOWN.

$$I_E = I_{E0}\left(e^{\frac{V_{BE}}{V_t}} - 1\right)$$

WHERE $V_t = \frac{kT}{q}$ (TEMPERATURE DEPENDENCE)

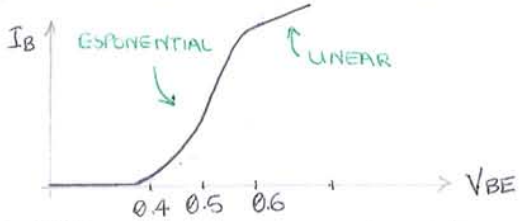

FIG A1.8 Input characteristic

THE DC EMITTER AND COLLECTOR CURRENTS IN ACTIVE MODE CAN BE MODELED BY THE EBERS-MOLL MODEL:

$$I_C \approx I_E = I_S \, e^{\frac{V_{BE}}{V_t}}$$

↑ α IS REALLY SMALL!

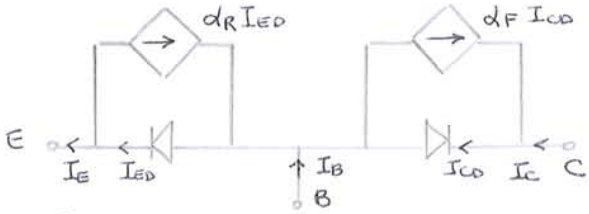

FIG A1.11 : Ebers-Moll model for a n-p-n BJT.

MOS

THE METAL OXIDE SEMICONDUCTOR TRANSISTOR IS A TYPE OF FET (FIELD EFFECT TRANSISTOR), SO NAMED BECAUSE OF THE VERTICAL SEQUENCE OF MATERIALS WHICH CONSTITUDESTHE GATE OF THE TRANSISTOR.

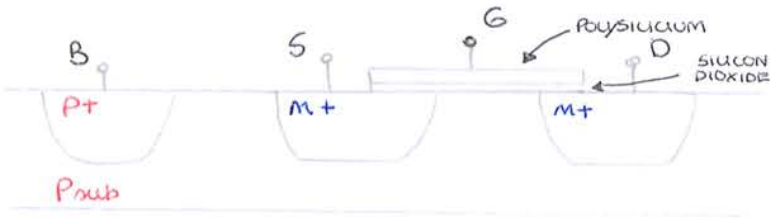

FIG A1.12 : N-MOS representation

CHARGE FLOW, IN A FET AND IN PARTICULAR IN A MOSFET, IS DUE TO THE INDUCTION OF A CHANNEL BETWEEN THE "POCKETS" OF DRAIN AND SOURCE THROUGH WHICH THE FLOW OF ELECTRONS (N-MOS) OR HOLES (P-MOS) OCCURS.
THIS CHANNEL IS INDUCED BY THE APPLICATION OF A SUITABLE VOLTAGE BETWEEN GAIN AND SOURCE. WHEN:

$$V_{GS} = V_{Tn} = V_{Tn}(t_{ox}, N_A),$$

WE CAN ASSUME THAT THE CHANNEL IS UNIFORM. IT'S COMPOSED OF MOBILE ELECTRONS.

SO, IF WE APPLY A $V_{DS} \neq 0$, THERE IS A CURRENT FLOW: ELECTRONS GO FROM SOURCE TO DRAIN.

FOR LOW VALUES OF V_{DS}, THE CHANNEL OFFERS A CONSTANT RESISTANCE TO THE CHARGE FLOW, BUT WHEN V_{DS} ↑ THIS RESISTANCE STARTS TO CHANGE. WHEN V_{DS} IS HIGHER THAN A FIXED VALUE, THE CHANNEL BREAKS UP AND IT'S LIKE IT OFFERED A NULL RESISTANCE TO THE CHARGE FLOW, WHICH IS STILL POSSIBLE BECAUSE OF THE INTENSE ELECTRIC FIELD WHICH IS RELEATED TO THE HIGH VALUE OF V_{DS}.

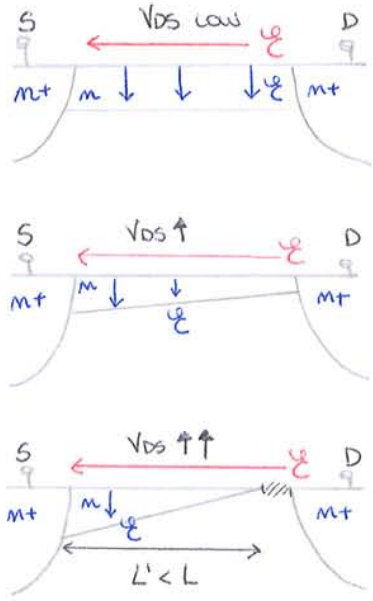

FIG A1.13 N-channel variations according to V_{DS} increasing

IN FIG A1.17 THE FAMILY OF OUTPUT CHARACTERISTICS OF A MOSFET, OBTAINED WHEN V_{GS} SWEEPS FROM V_{TH} TO ITS MAXIMUM VALUE, IS SHOWN. WE CAN IDENTIFY SOME DISTINCT REGIONS OF OPERATION, DEFINED BY THE EFFECT OF A DIFFERENT V_{DS} ON THE CHANNEL.

FIG A1.17: Output characteristic curves

WHERE

- $V_{GS} < V_{TH} \rightarrow I_D = 0A \Rightarrow$ CUT OFF REGION
- $V_{DS} < 2(V_{GS} - V_{TH}) \rightarrow I_D = K[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \Rightarrow$ RESISTIVE REGION
- $V_{DS} = 2(V_{GS} - V_{TH}) \rightarrow I_D = K(V_{GS} - V_{TH})^2 \Rightarrow$ PINCH-OFF
- $V_{DS} > 2(V_{GS} - V_{TH}) \rightarrow I_D = K2(V_{GS} - V_{TH})V_{DS} \Rightarrow$ SATURATION REGION

K IS THE TRANSCONDUCTANCE OF THE PROCESS AND IT'S EQUAL TO:

$$K = \frac{\mu_x \cdot C_{ox}}{2} \cdot \frac{W}{L}$$

WHERE

- μ_x IS THE ELECTRON MOBILITY (HOLE MOBILITY) → P OR N
- C_{ox} IS THE CAPACITANCE OF THE SiO_2 FOR UNIT OF AREA
- W IS THE CHANNEL WIDTH
- L IS THE CHANNEL LENGTH

FOR MOSFET WE HAVE AN EFFECT SIMILAR TO THE "EARLY EFFECT" DUE TO THE REDUCTION OF THE EFFECTIVE CHANNEL LENGTH.

WE CAN EVALUATE THE POWER AS:

$$P_D = I_D \cdot V_{DS} = I_D (V_{DD} - I_D R_D)$$

WHERE

$$V_{DS|max} = V_{DD}/2$$

AS HAPPENS FOR BJT, THE POWER CURVE HAS A PARABOLIC ANDAMENT.

AMPLIFIERS

- TYPES
- GAIN
- LINEARITY
- EFFICIENCY
- BANDWIDTH
- NOISE
- SLEW RATE
- DYNAMIC RANGE
- EQUIVALENT MODEL
- OP AMP

④ LINEARITY ⇒ IT'S THE DEGREE OF PROPORTIONALITY BETWEEN INPUT AND OUTPUT.

IF WE COMPARE AN IDEAL AND A REAL TRANSCHARACTERISTIC, WE CAN SEE THAT THEY'RE DIFFERENT BECAUSE THE REAL ONE IS NON LINEAR OR LINEAR ONLY IN A LIMITED RANGE. THE BEHAVIOR OF THE DEVICE IN THIS LIMITED LINEAR RANGE CAN BE DESCRIBED BY USING EQUIVALENT MODELS; WHILE IN ORDER TO DESCRIBE THE BEHAVIOR OF THE DEVICE IN NON LINEAR RANGE WE NEED TO STUDY THE CAUSES WHICH ESSENTIALLY ARE LINKED TO THE APPLICATION OF LARGE SIGNALS. THE NON-LINEARITY CAUSES HARMONIC DISTORSION IN THE OUTPUT.

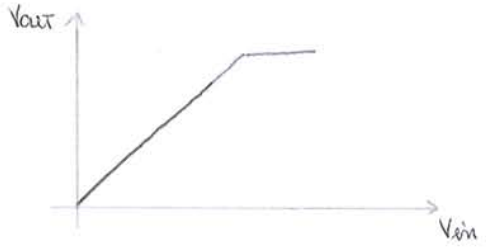

FIG A2.2 Ideal transchoracteristic

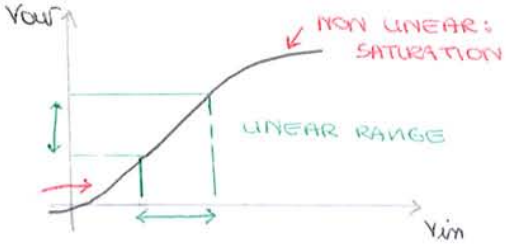

FIG A2.3 Real transchoracteristic

⑤ NOISE ⇒ IT'S A MEASURE OF UNDESIRED NOISE MIXED INTO THE OUTPUT. EVERY SIGNAL IS AFFECTED BY NOISE AND EVERY ELECTRONIC SYSTEM INTRODUCES NOISE.

THE PROBLEM IS THAT THE AMPLIFIER AMPLIFIES THE NOISE TOO. IF THE AMPLIFIER IS A DC AMPLIFIER, THE LEVEL OF THE NOISE COULD BE COMPARABLE WITH THE LEVEL OF THE INPUT SIGNAL AND THAT'S A PROBLEM. FOR THIS REASON, DC AMPLIFIERS MUST BE LOW NOISE AMPLIFIERS!

THE NOISE PERFORMANCE IS QUANTIFIED BY THE SIGNAL-TO-NOISE POWER RATIO:

$$SNR = \frac{\text{POWER OF THE FONDAMENTAL HARMONIC}}{\text{POWER OF NOISE (EXCLUDING DC)}} = \frac{P_F}{P_N}$$

IN RADIO SYSTEM, ANOTHER VERY USED PARAMETER IS:

$$SINAD = \frac{P_F}{P_N + P_{DC}} \quad \text{(INCLUDING DC)}$$

NOTE: WHEN WE EXPRESS SNR OR SINAD IN dB, WE'VE TO WRITE:

$SNR(dB) = 10\log(SNR)$ because it's a POWER RATIO

⑥ OUTPUT DYNAMIC RANGE ⇒ IT'S THE RATIO OF THE LARGEST AND THE SMALLEST USEFUL OUTPUT LEVELS.

⑦ SLEW RATE ⇒ IT'S THE MAXIMUM VELOCITY OF CHANGE OF THE OUTPUT LINKED TO THE RATE OF CHANGE OF THE INPUT.

IF WE REPEAT THESE CONSIDERATIONS FOR THE OTHER TYPES OF AMPLIFIERS, WE CAN FIND OUT THAT, IN ORDER TO HAVE AN HIGH GAIN, THE INPUT AND OUTPUT EQUIVALENT IMPEDANCES (RESISTANCES IF THERE ARE NO LOSSESS) SHOULD BE:

	VOLTAGE A.	CURRENT A.	TRANSCONDUCTANCE A.	TRANSRESISTANCE A.
Z_{in}	HIGH	LOW	HIGH	LOW
Z_{out}	LOW	HIGH	HIGH	LOW

HOW CAN WE REALIZE AN AMPLIFIER?

THERE ARE SEVERAL WAYS TO REALIZE AN AMPLIFIER; THE DESIGN AND THE COMPONENTS ARE CHOSEN ACCORDING TO THE SPECIFICATIONS OF THE PROJECT.

- OP AMP (THEY'LL BE ANALIZE LATER IN A DEGRESSION)
- BJT AND MOSFET CAN BE USED AS AMPLIFIERS IF THEY'RE FORCED TO WORK IN RAD AND SATURATION REGION RESPECTIVELY. IN THESE REGIONS, IN FACT, THE OUTPUT CURRENT IS NEARLY CONSTANT AND IT CAN BE CONTROLLED BY THE INPUT CURRENT OF VOLTAGE RESPECTIVELY.

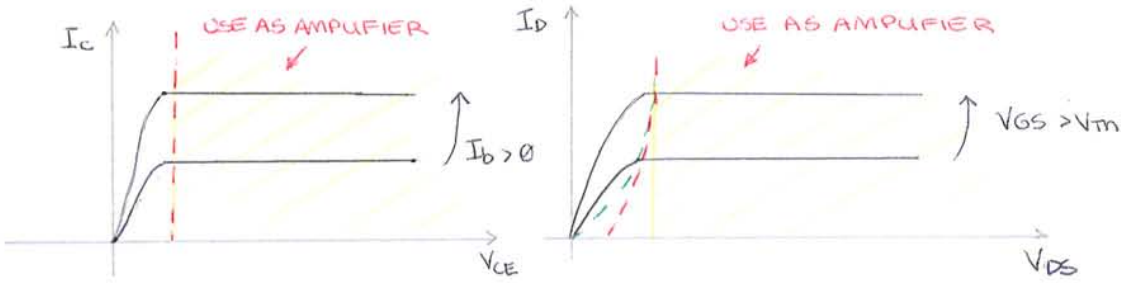

FIG A2.7: operating region as amplifier for BJT and MOSFET

IN REALITY THERE ARE ALSO OTHER OPERATIONAL LIMITS TO BE OBSERVED, CONCERNING THE LEVEL OF VOLTAGE AND CURRENT AND THE DISSIPATED POWER. THE ACTIVE & SAFE OPERATING AREA (SOA) FOR A MOSFET IS SHOWN IN FIG A2.8

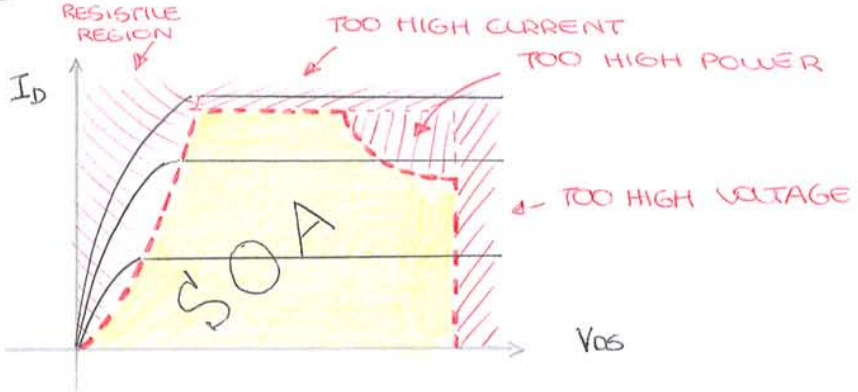

FIG A2.8 SOA (Save and operating area)

WE CAN CONSIDER TWO BASIC OP AMP CONFIGURATIONS:

OPEN LOOP:
THE VALUE OF A_V IS VERY HIGH AND IT CAN'T BE CONTROLLED, SO THIS CONFIGURATION IS IMPRATICAL TO BE USED AS AMPLIFIER.
IT CAN BE USED AS **COMPARATOR**.

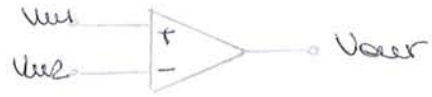

FIG A2.11 Open loop conf.

CLOSED LOOP:
THE FEEDBACK ALLOWS A BETTER CONTROL OF THE GAIN. IT MUST BE NEGATIVE BECAUSE A POSITIVE FEEDBACK BRINGS THE OUTPUT INTO SATURATION AND THE DEVICE INTO DAMAGE.

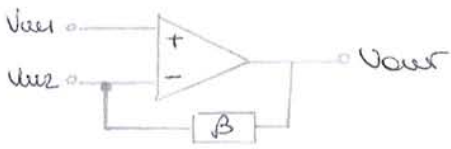

FIG A2.12 Closed loop conf. (negative feedback)

IN GENERAL, IF WE SCHEMATIZE THE OP AMP WITH A BLOCK A AND THE FEEDBACK WITH A BLOCK β, WE'VE:

$$\begin{cases} V_{out} = A \cdot V_x \\ V_x = V_{in} - \beta \cdot V_{out} = V_{in}(1 - A\beta) \end{cases}$$

$$A_{TOT} = \frac{V_{out}}{V_{in}} = \frac{A}{1 - A\beta}$$

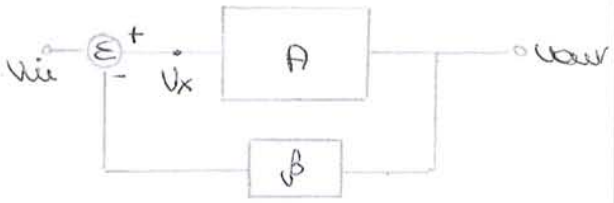

FIG A2.13 Feedback

WE CAN HAVE TWO CONFIGURATIONS:

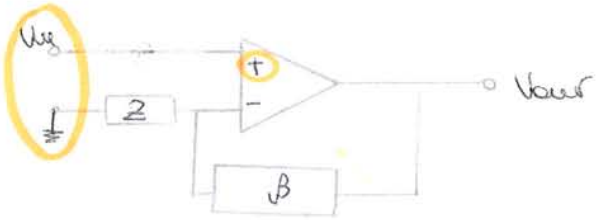

FIG A2.14 Non inverting configuration

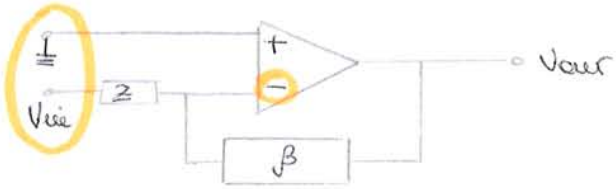

FIG A2.15 Inverting configuration

ACCORDING TO THE FEEDBACK UNIT, WE OBTAIN DIFFERENT TYPES OF OP AMP APPLICATION. MOST OF THEM ARE BASED ON INVERTING CONFIGURATION BECAUSE IT'S EASIER TO REALIZE AND CONTROL.
SO, FIRST OF ALL, LET'S GO TO ANALYZE STANDARD INVERTING AND NON INVERTING CONFIGURATIONS (RESISTIVE FEEDBACK LOOP).

NON INVERTING CONFIGURATION

- V_{in} AND V_{out} ARE IN PHASE
- R_1 AND R_2 ARE IN SERIES

$$A = \frac{V_{out}}{V_{in}} = \frac{V(R_1) + V(R_2)}{V_{in}} =$$

$$= \frac{V_{in} + V_{in}\left(\frac{R_2}{R_1}\right)}{V_{in}} = 1 + \frac{R_2}{R_1}$$

$$V_m = V_{out} \cdot \frac{R_1}{R_1 + R_2}$$

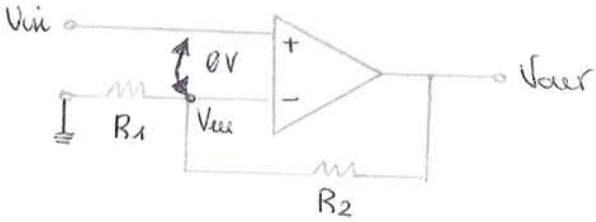

FIG A2.16 Non inverting configur.

(5) LET'S ANALYZE IN MORE DETAIL THE **INTEGRATOR CONFIGURATION**.

THE IDEAL INTEGRATOR IS SHOWN IN FIG A2.20, WHILE THE REAL INTEGRATOR IN FIG A2.21. THE DIFFERENCE BETWEEN THE TWO CONFIGURATIONS CONSISTS IN THE PRESENCE OF A RESISTANCE IN PARALLEL TO THE CAPACITOR.

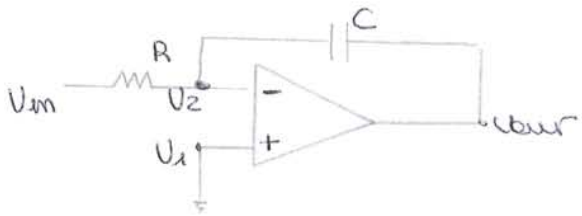

FIG A2.20 Ideal active integrator

THIS RESISTANCE ALLOWS TO DEAL WITH THIS CIRCUIT EVEN AT QUASI-DC FREQUENCIES: AT THESE LOW FREQUENCIES, IN FACT, THE CAPACITOR BECAMES AN OPEN CIRCUIT AND THE LOOP IS OPEN, LEADING TO OPAMP SATURATION AT OUTPUT.

IF WE PUT A RESISTANCE IN PARALLEL, AT LOW FREQUENCIES THE SIGNAL PASSES TROUGH THE RESISTANCE AND THE OPAMP IS IN A STANDARD INVERTING CONFIGURATION.

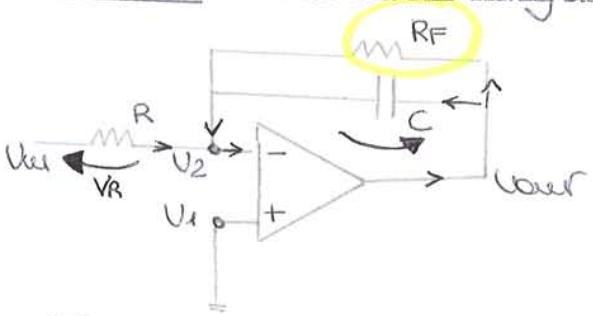

FIG A2.21 Real active integrator

MATHEMATICALLY SPEAKING, WE'VE:

$$I_C = C \cdot \frac{dV_C}{dt} = C \frac{d(V_2 + V_{out})}{dt} = C \cdot \frac{dV_{out}}{dt}$$

$V_2 = 0$ for the virtual short!

$$I_R = \frac{V_{in} - V_2}{R} = \frac{V_{in}}{R}$$

AND SO:

$$\frac{V_{in}}{R} = C \frac{dV_{out}}{dt} \Rightarrow V_{out} = \frac{1}{RC} \int V_{in}\, dt$$

THE FREQUENCY RESPONSE OF THE INTEGRATOR IS SHOWN IN FIG A2.22: WE CAN NOTICE A **POLE INTO THE ORIGIN**. THE **CUT OFF FREQUENCY** IS:

$$f_C = \frac{1}{2\pi} \cdot \frac{1}{R_F C}$$

WHILE THE CROSSOVER FREQUENCY IS:

$$f_B = \frac{1}{2\pi} \cdot \frac{1}{RC}$$

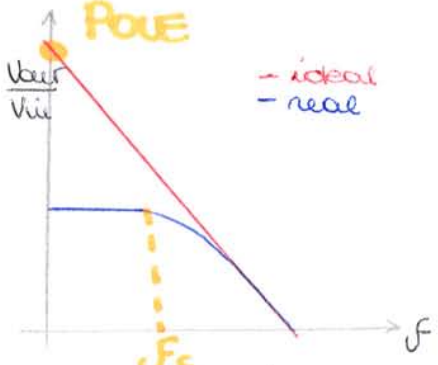

FIG A2.22 Bode diagram

(4) WE CAN OBTAIN A DERIVATOR JUST BY INVERTING THE POSITION OF R AND C.

LESSON: 6
DATE: 10-03-16
PROF: D. DEL CORSO

A3: BJT AMPLIFIERS

THE ANALYSIS OF BJT AMPLIFIERS PASSES THROUGH THE FOLLOWING STEPS:

1. BIASING;
2. OUTPUT DYNAMIC RANGE;
3. SMALL SIGNALS ANALYSIS;
4. VOLTAGE GAIN;
5. FREQUENCY RESPONSE.

WE'LL ANALYZE THEM IN DETAIL.

1) BIASING

IN ORDER TO USE THE BJT AS AN AMPLIFIER, IT MUST WORK IN THE RAD (DIRECTIVE ACTIVE REGION). TO ENSURE THIS, WE CAN DESIGN A BIAS CIRCUIT (IE USUALLY A RESISTIVE NETWORKS) WHICH FORCES A SPECIFIC DC COLLECTOR CURRENT. THIS CURRENT, THAT WILL BE INDICATED AS I_C^* IN THE FOLLOWING, HAS A GREAT INFLUENCE ON THE BEHAVIOR OF THE BJT AS AMPLIFIERS, SO IT SHOULD NOT BE AFFECTED BY THE VARIATIONS OF β, OF THE TEMPERATURE AND SO ON.
ONE OF THE MOST USED BIAS CIRCUIT IS SHOWN IN FIG. A3.1.

IF WE ASSUME THAT:

- h_{FE} $(= \beta_F = I_C/I_B)$ IS ELEVATED
- $I_1 \gg I_B$

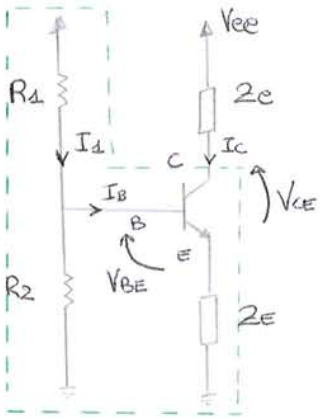

FIG A3.1 Bias circuit

WE CAN WRITE THAT, WITH A REASONABLE GRADE OF APPROXIMATION:

$$I_C \approx I_E = \frac{V_B - V_{BE}}{R_E}$$

$$V_B \approx V_{BB} = V_{ee} \cdot \frac{R_2}{R_1 + R_2}$$

WHERE, SINCE THE BJT MUST WORK IN RAD, $V_{BE} = 0.6\ V$
WHILE V_{BB} CAN BE EVALUATED USING THE THEVENIN EQUIVALENT CIRCUIT IN FIG A3.2, WHERE

$$R_B = R_1 // R_2 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$

$$V_{BB} = V_{ee} \cdot \frac{R_2}{R_1 + R_2}$$

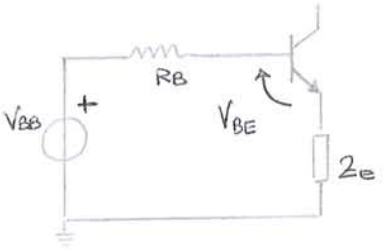

FIG A3.2 Equivalent Thevenin circuit

NOTE THAT ONLY THE DASHED MESH IN FIG A3.1 GIVES A CONTRIBUTE IN THE EVALUATION OF THE BIAS POINT.
THE VALUE OF 2_C CAN BE USED TO SATISFY A SPECIFICATION ABOUT THE OUTPUT RANGE, BUT WE WILL TALK ABOUT THIS IN THE NEXT STEP.

③ SMALL SIGNALS ANALYSIS

FOR "SMALL SIGNAL" WE MEAN A SIGNAL WHICHIS THE SMALLER AS POSSIBLE, BUT THERE ARE NOT SPECIFIC REFERENCES.
WE CAN ASSUME THAT IF

$$V_{BE} \ll V_t \approx 26\,mV \quad (\text{FOR } T = 300K)$$

- mV IS A GOOD AMPLITUDE FOR LINEARITY.
- μV ISN'T BECAUSE IT'S COMPARABLE WITH NOISE.

WE CAN APPROXIMATE THE ESPONENTIAL RELATION BETWEEN I_C AND I_S TO A LINEAR ONE:

$$I_C \cong I_E = I_S e^{\frac{V_{BE}}{V_t}} \approx I_S \left(1 + \frac{V_{BE}}{V_t}\right)$$

REMIND:
$e^x \approx 1 + x$
WHEN $x \ll 1$

IN THIS HYPOTHESIS, WE HAVE THAT THE BEHAVIOUR OF THE BJT CAN BE MODELED BY AN EQUIVALENT CIRCUIT, SHOWN IN FIG A3.4, WHOSE CHARACTERISTIC PARAMETERS ARE:

- $g_m = \frac{I_C^*}{V_t}$ TRANS CONDUCTANCE
- $h_{FE} = \beta_F$
- $h_{IE} = h_{FE} \cdot \frac{V_t}{I_C^*} = \frac{h_{FE}}{g_m}$

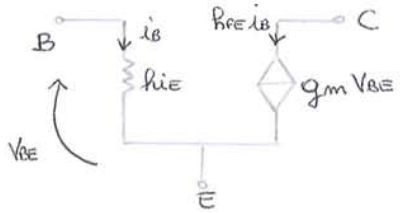

FIG A3.4 Small signal model

④ VOLTAGE GAIN

THE VOLTAGE GAIN CAN BE COMPUTED USING THE LINEAR MODEL.
BEFORE STARTING THE ANALYSIS, WE HAVE TO DECIDE A CONFIGURATION FOR THE AMPLIFIER BETWEEN:

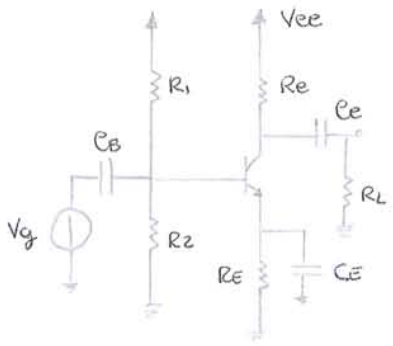

FIG A3.5 Common Emitter configuration

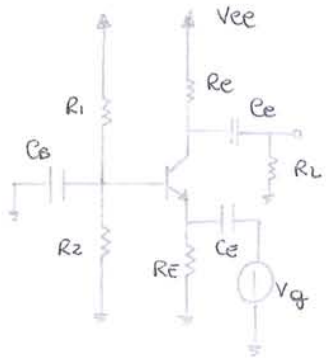

FIG A3.6 Common Base configuration

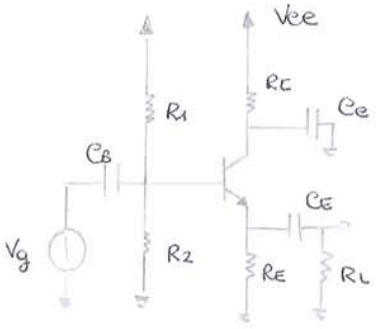

FIG A3.7 Common Collector configuration

R_{in} = LOW
R_{out} = HIGH
$|A_V| \gg 1$
$A_i \gg 1$

← VOLTAGE GAIN →

R_{in} = LOW
R_{out} = HIGH
$A_V \gg 1$
$A_i \approx 1$

CURRENT GAIN →

R_{in} = HIGH
R_{out} = LOW
$A_V \approx 1$
$A_i \gg 1$

(5) FREQUENCY RESPONSE

THE FREQUENCY RESPONSE IS DETERMINATED BY THE PRESENCE OF THE CAPACITANS, IN PARTICULAR

- THE LOW FREQUENCY LIMIT => DEPENDS BY C_B, C_E AND C_C.
- THE HIGH FREQUENCY LIMIT => DEPENDS BY C_3 WHICH IS LINKED TO A SERIES OF PARASITIC EFFECTS WHICH CAN'T BE NEGLIGED AT HIGH FREQUENCY.

THE PARASTITIC CAPACITANCES MODEL THE EFFECT OF THE NON-INSTANTANEOUS CHARGE REDISTRIBUTION BETWEEN BJT'S JUNCTIONS, SO THERE ARE 3 PARASTITICS CAPACITANCES THAT WE HAVE TO TAKE IN ACCOUNT OF. IN PARTICULAR, C_{BC} SUFFERS OF THE MILLER EFFECT.
AMONG C_B, C_e, C_E WE CAN CHOSE ONE OF THEM AS RESPONSABLE OF THE LOWER BANDWIDTH LIMIT (USUALLY WE CHOSE THE ONE WHICH OPERATES IN BETTER DEFINED CONDITIONS); THE OTHER TWO CAPACITORS ARE CHOSEN IN A WAY THAT THEY INTRODUCE POLES ONLY IN LOWER FREQUENCIES.

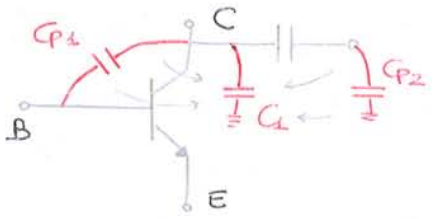

FIG A3.10 Parasitic capacitances synthesized in C_L.

THE TIME CONSTANTS ASSOCIATED TO EACH CAPACITY ARE:

$$\tau_B = C_B \cdot [R_B // (R_{iE} + (\beta_F + 1) R_{E1})]$$
$$\tau_E = C_E \cdot (R_{E1} // R_{E2})$$
$$\tau_C = C_C \cdot (R_L + R_C)$$
$$\tau_1 = C_L (R_L // R_e)$$

WE OBTAIN A FREQUENCY RESPONSE WHICH IS SOMETHING SIMILAR TO WHAT IS REPRESENTED IN FIG. A3.11, BLACK LINE.
ACTUALLY WE HAVE TO TAKE INTO ACCOUNT OF ERRORS ABOUT

- BANDWIDTH (HORIZONTAL DISCREPANCES)
- VALUES (VERTICAL DISCREPANCES)

SO EVERY "POINT" ON THE GRAPH IS "CONTAINED" INTO A RECTANGLE DEFINED BY THE MAXIMUM VALUES OF ADMITTED ERRORS (USUALLY ABOUT 2-5%).
WE HAVE TO TAKE INTO ACCOUNT OF THIS WHEN WE HAVE TO SATISFY SPECIFICATIONS.

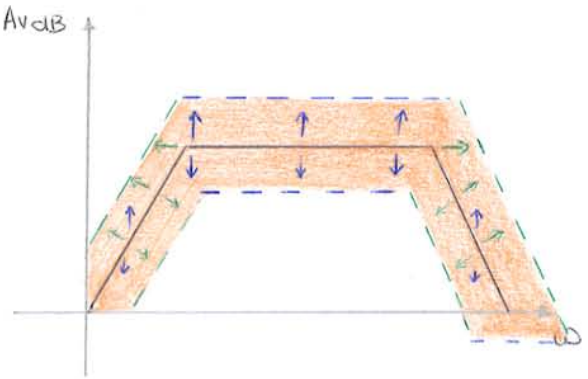

FIG A3.11 Mask (DEFINED BY THE % OF ERROR)

WE CAN IMPROVE THE BANDWIDTH USING A CASCODE CONFIGURATION, WHICH REDUCES PARASITIC EFFECTS. IN PARTICULAR, C_{BC} IS NO MORE EFFECTED BY MILLER EFFECT.

CASCODE CONFIGURATION PRESENTS AN AMPLIFIER FOLLOWED BY A CURRENT BUFFER USUALLY ONE STADIUM IS OPERATING AS COMMON EMITTER AND ONE OTHER AS COMMON BASE, IN THIS WAY THE INPUT-OUTPUT ISOLATION IS IMPROVED BECAUSE THERE'S NO DIRECT COUPLING BETWEEN INPUT AND OUTPUT, AND THE MILLER EFFECT IS ELIMINATED.

← COMMON BASE, $A_I \approx 1$!!

HOWEVER, THIS CONFIGURATION REQUIRES AN ADDITIONAL VOLTAGE DROP ON Q2 SO AN HIGHER POWER SUPPLY IS REQUIRED.

→ THAT'S WHY THIS CONFIGURATION IS USUALLY REPLACED BY A DIFFERENTIAL CONFIGURATION.

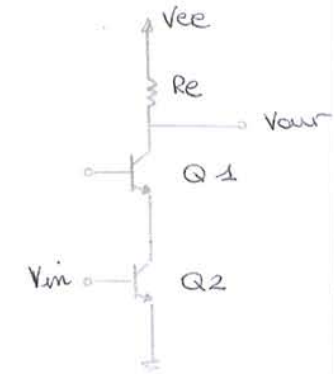

FIG A3.12 Cascode configuration

DIGRESSION

A DIFFERENTIAL AMPLIFIER IS A TYPE OF ELECTRONIC AMPLIFIER THAT AMPLIFIES THE DIFFERENCE BETWEEN TWO VOLTAGES BUT DOES NOT AMPLIFY THE PARTICULAR VOLTAGE. ITS SYMBOL AND COMPLETE STRUCTURE ARE SHOWN IN FIG. A3.14 AND A3.15 RESPECTIVELY.
THE DIFFERENTIAL GAIN IS DEFINED AS:

$$A_d = \frac{V_{out2} - V_{out1}}{V_{in2} - V_{in1}}$$

WHEN $R_{C1} = R_{C2}$, $A_{dl} = -g_m R_C$:
THE DIFFERENTIAL AMPLIFIER HAS A BEHAVIOUR SIMILAR TO THE COMMON-E. AMPLIFIER.

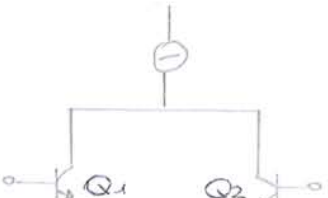

FIG A3.13 Differential configuration

IN PRACTICE, HOWEVER, THE GAIN IS NOT QUITE EQUAL FOR THE TWO INPUTS; THIS MEANS, FOR INSTANCE, THAT IF V_{in1} AND V_{in2} ARE EQUAL, THE OUTPUT WILL NOT BE ZERO.
THAT'S WHY THERE IS AN ADDICTILE COMPONENT AT THE OUTPUT WHICH IS CALLED COMMON-MODE GAIN OF THE AMPLIFIER AND IS DEFINED AS:

$$A_C = \frac{V_{out2} - V_{out1}}{\left(\frac{V_{in1} + V_{in2}}{2}\right)}$$

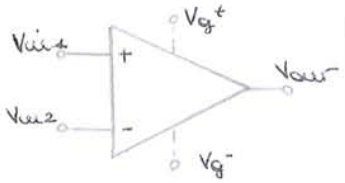

FIG A3.14 Differential amplifier's symbol

SINCE A DIFFERENTIAL AMPLIFIER IS OFTEN USED TO NULL OUT NOISE OR BIAS VOLTAGES THAT APPEAR IN BOTH INPUTS, A LOW COMMON MODE GAIN IS USUALLY DESIRED.
THE COMMON MODE REJECTION RATIO INDICATES THE ABILITY OF THE AMPLIFIER TO CANCEL VOLTAGES THAT ARE COMMON TO BOTH INPUTS AND IT'S DEFINED AS:

$$CMRR = 20 \log\left(\frac{A_d}{A_C}\right)$$

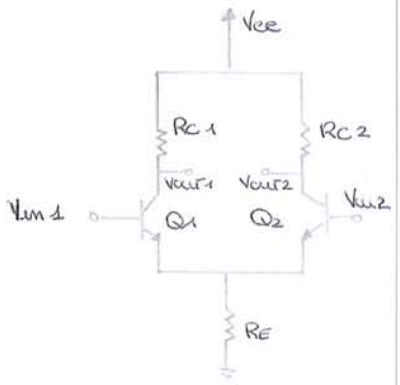

FIG A3.15 Differential configuration

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LESSON: 5
DATE: 12-03-16
PROF: D. DEL CORSO

A4: MOS AMPLIFIERS

THE ANALYSIS OF MOSFET AMPLIFIERS IS QUITE SIMILAR TO THE ONE CONDUCED FOR BJT AMPLIFIERS, SO WE WILL GIVE ONLY SOME INFORMATIONS ABOUT THE CHARACTERISTICS WHICH ARE DIFFERENT FROM BJT ANALYSIS.

① BIASING

THE MOSFET MUST BE FORCED TO WORK IN SATURATION REGION, SO A BIAS ANALYSIS IS NECESSARY. WE CAN USE THE SAME BIAS CIRCUITS INTRODUCED FOR BJT AMPLIFIERS.

② OUTPUT DYNAMIC RANGE

$$V_{out} = V_{DD} - R_D I_D = V_{DS} + R_S I_S$$

$$V_{out}|_{max} = V_{out}|_{I_D=0} = V_{DD}$$

$$V_{out}|_{min} = V_{out}|_{V_{DS}=min} = V_{TH} + R_S I_S$$

So $\Delta V_{out}|_{no\ load} = V_{DD} - V_{TH} - R_S I_S$

③ SMALL SIGNALS ANALYSIS

IF WE DEAL WITH SMALL SIGNALS, WHICH IN THIS CASE ARE SUCH THAT:

$$V_{gs} \ll 2\,(V_{GS} - V_{TH})$$

WE CAN APPROXIMATE THE QUADRATIC RELATION BETWEEN I_D AND V_{GS} WITH A LINEAR ONE. NOTE THAT THIS APPROXIMATION IS LOWER THAN THE ONE DID FOR BJT

THE MOS SMALL SIGNAL MODEL IS VERY SIMILAR TO THE ONE INTRODUCED FOR BJT AND IT'S SHOWN IN FIG A4.1. NOTE THE ASSENCE OF R_{ie} DUE TO THE FACT THAT THERE'S NO CURRENT IN THE G.

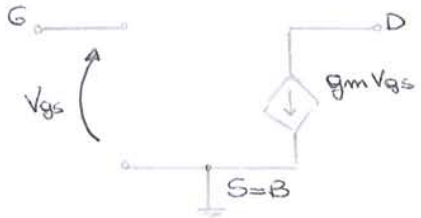


FIG A4.1: Linear model

THE CHARACTERISTIC PARAMETER

$$g_m = \underbrace{\mu_n \cdot C_{ox} \cdot \frac{W}{L}}_{2K} (V_{GS}^{*} - V_{TH})$$

④ VOLTAGE GAIN

ALSO THIS TIME WE'LE SEVERAL CONFIGURATIONS WHOSE CHARACTERISTICS ARE SIMILAR TO THE ONES INTRODUCED DURING THE BJT AMPLIFIERS' ANALYSIS.

COMMON E. ⇒ COMMON S.
COMMON B. ⇒ COMMON G.
COMMON C. ⇒ COMMON D.

SO FOR A COMMON S. STAGE, WE CAN EASY EVALUATE THE GAIN AS:

$$A_V = \frac{\partial V_{out}}{\partial V_{in}} = \frac{\partial}{\partial V_{in}}(V_{DD} - R_D I_D) = \frac{\partial}{\partial V_{in}}(V_{DD} - R_D \cdot (K \cdot (V_{GS} - V_{TH})^2)) =$$

(SATURATION REGION!)

$$= \frac{\partial}{\partial V_{in}}(V_{DD} - R_D (K (V_{in} - V_{TH})^2)) = -R_D \cdot K (V_{in} - V_{TH}) 2 =$$

$$= -R_D \cdot g_m$$

NOTE: IF WE LOOK AT THE I/O CHARACTERISTIC, SHOWN IN FIG AG.2, WE CAN SEE THAT V_{out} ↓ WHEN V_{in} ↑, UNTIL A VALUE WHICH IS ≠0 BECAUSE OF THE PRESENCE OF A LOAD. THE SLOPE OF THE CURVE IS NEGATIVE (IN FACT THE GAIN IS NEGATIVE) AND DEPENDS BY R_D.

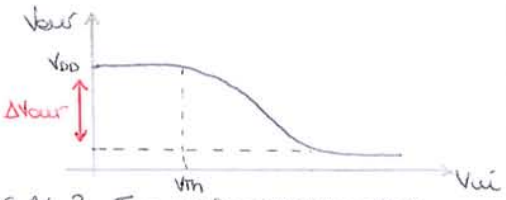


FIG AG.2 Transcharacteristic

- IF WE INCREASE R_D ⇒ A_V ↓, ΔV_{out} ↑
- IF WE DECREASE R_D ⇒ A_V ↑, ΔV_{out} ↓

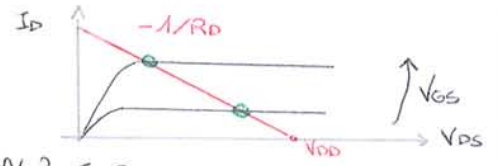


FIG AG.3 Intersection of MOS characteristics and load line.

THERE ARE OTHER TECNIQUES THAT ALLOW US TO INCREASE THE GAIN:

- TO INCREASE POWER SUPPLY V_{DD} ⇒ IT'S NOT A GOOD IDEA BECAUSE P_d ↑
- TO USE A CURRENT GENERATOR ⇒ WHOSE CHARACTERISTIC IS A CONSTANT LINE
  - HOW CAN WE REALIZE A CURRENT GENERATOR?
    - ANOTHER TRANSISTOR WITH FIXED V_{GS}
    - A CURRENT MIRROR

FIG. AG.4 Intersection of MOS characteristic and another MOS with fixed VGS characteristic

ALL THESE CONSIDERATION COULD HAVE BEEN DONE ALSO FOR BJT, BUT REFFERING TO A MOS IT'S EASIER TO DO A GRAPHICAL ANALYSIS.

DIGRESSION

A CURRENT MIRROR IS A CIRCUIT DESIGNED TO COPY A CURRENT THROUGH ONE ACTIVE DEVICE BY CONTROLLING THE CURRENT IN ANOTHER ACTIVE DEVICE OF A CIRCUIT, KEEPING THE OUTPUT CURRENT CONSTANT REGARDLESS OF LOADING. IT'S A SIMPLY AND IDEAL INVERTING CURRENT AMPLIFIER THAT REVERSES THE CURRENT DIRECTION AS WELL OR IT'S A CURRENT CONTROLED CURRENT SOURCE. IT'S OFTEN USED TO PROVIDE BIAS CURRENTS AND ACTIVE LOADS TO THE CIRCUIT.

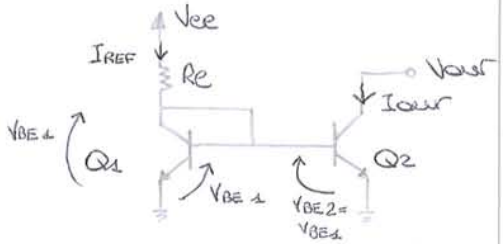


FIG AG.5 Current mirror

AS WE CAN SEE IN FIG AG.5, Q1 AND Q2 ARE MATCHED.

$$I_{out} = I_C^* = I_{REF} \cdot \frac{\beta_F}{\beta_F + 2}$$

RADIO FREQUENCY ARCHITECTURE

- RECEIVER (GENERALITIES)
- FILTER
  - LC TUNED CIRCUITS
  - MECHANICAL FILTERS
  - SWITCHED CAPACITORS
  - DIGITAL FILTERS
- HETERODYNE
- IMAGE PROBLEM
  - DUAL CONVERSION FREQUENCY
  - I/Q PROCESSING
    - STANDARD
    - HEARTLY REJECTION MIXER
- AMPLIFIERS
- DEMODULATION
  - ANALOG
  - DIGITAL
- TRANSMITTER

FIGB1.3 Tx antenna

THE INPUT SIGNAL IS TRANSMITTED BY AN **ANTENNA**. IT CONTAINS THE WANTED INFORMATION PLUS MANY TYPES OF NOISE AND INTERFERENCES, SO WE NEED TO **SELECT AND ISOLATE THE SIGNAL WE'RE INTERESTED IN** AND TO EXTRACT THE INFORMATION WE WANT FROM IT. IN ORDER TO DO THIS, WE NEED THAT THE LEVEL OF THE SIGNAL IS ELEVATED ENOUGH TO DRIVE TRANSDUCER. USUALLY, ELECTRICAL SIGNALS COLLECTED BY THE ANTENNA MAY HAVE VERY LOW LEVELS (~μV) SO WE NEED TO AMPLIFY THEM.

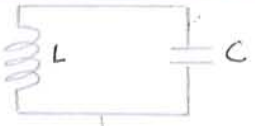
SO, A **RECEIVER** MUST:

- **SELECT A CHANNEL** (= A RANGE OF FREQUENCY) FROM THE SOURCE (THE AIR)
  - → FILTER (NARROW BAND OR BAND-PASS)
- **AMPLIFY THE SIGNAL**
  - → AMPLIFIER (LOW-NOISE AMPLIFIER)
- **TRANSLATE THE SIGNAL IN SOMETHING USEFUL BY HUMAN** (IE SOUNDS)
  - → DEMODULATOR

LET'S SEE HOW WE CAN REALIZE THESE DEVICES.

FILTER: **WE NEED A NARROW BAND FILTER IN ORDER TO SELECT A CHANNEL, PLUS WE NEED A FILTER WHOSE CUT OFF FREQUENCY CAN BE VARIED ACCORDING TO THE CHANNEL WE WANT TO SELECT.**

① THE EASIEST WAY TO REALIZE A FILTER IS USING A **TUNED CIRCUIT**: WE CAN CHANGE f_c CHANGING THE VALUES OF L AND C.

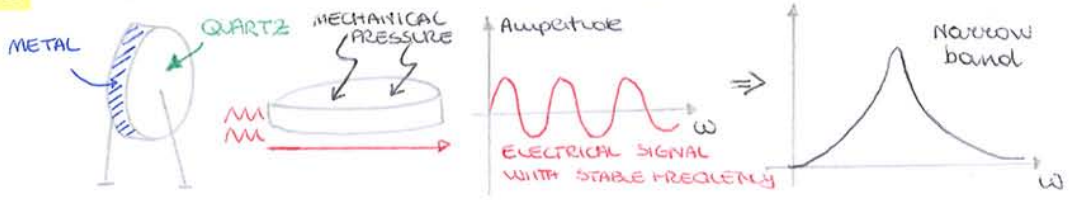


FIGB1.4 Tuned circuit

WE CAN CHANGE C BY:
- VARYING THE THICKNESS OR THE AREA
- INVERTING DC VOLTAGE

WE CAN CHANGE L BY:
- VARYING THE LENGTH OF THE COIL
- INSERTING A FERRITE BLOCK IN THE WINDING

② ANOTHER TECHNIQUE TO REALIZE FILTERS IS THE USE OF **SAW** (SURFACE ACOUSTIC WAVE). THIS TECHNIQUE **CONVERTS ELECTRICAL SIGNALS TO MECHANICAL WAVES** IN A DEVICE CONSTRUCTED OF A PIEZOELECTRIC CRYSTAL OR CERAMIC; THESE WAVES ARE DELAYED AS THEY PROPAGATE ACROSS THE DEVICE. THEY ARE RECONVERTED INTO AN ELECTRICAL SIGNAL BY FURTHER ELECTRODES AND ASSUME THE ANALOG IMPLEMENTATION OF A FINITE IMPULSE RESPONSE FILTER.
THEY ARE LIMITED TO FREQUENCIES UP TO 3 GHz.
SAWS USE CERAMIC MATERIALS BECAUSE THEY ARE LESS EXPENSIVE.
THERE IS ALSO ANOTHER TYPE OF MATERIAL, THE **QUARTZ**, WHICH PRODUCES A VERY STABLE FREQUENCY ELECTRICAL SIGNAL WHEN WE APPLY A MECHANICAL PRESSURE ON IT. HOWEVER IT'S **VERY EXPENSIVE** AND IT'S USED WHEN WE NEED A VERY **PRECISE** FILTER OR A PRECISE OSCILLATOR (IE. MOBILE PHONES).



FIGB1.5 By left: quartz oscillator; application of a mechanical pressure which generates an electrical signal with a very stable frequency; obtained narrow band filter.

③ SWITCHED CAPACITOR FILTERS DEPEND ONLY ON THE RATIO BETWEEN CAPACITANCES AND THIS MAKES THEM MUCH MORE **SUITABLE FOR USE WITHIN IC** (INTEGRATED CIRCUIT), WHERE ACCURATELY RESISTORS AND CAPACITORS ARE NOT EASY AND ECONOMICAL TO CONSTRUCT.

④ DIGITAL FILTERS ALLOW A **BETTER CONTROL OF PARAMETERS BUT HAVE SOME LIMITS** AS FOR EXAMPLE POWER LIMITS.

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ALL THESE TYPES OF FILTER ARE GOOD BUT THEY ARE NOT SUITABLE FOR THE APPLICATION WE NEED: DESIGNING A FILTER WITH SHIFTING FREQUENCY AND NARROW BAND IS REALLY HARD.
THE BASIC IDEA THAT CAN RESOLVE OUR ISOLATION PROBLEM IS THE USE OF AN HETERODYNE ARCHITECTURE, LIKE THE ONE WHICH IS REPRESENTED IN FIG B1.1 AND THAT WE'RE GOING TO ANALYZE STEP BY STEP.

FIG B1.6: Wideband input filter

THE WIDEBAND INPUT FILTER IS A **BAND PASS FILTER** (WE CAN UNDERSTAN IT LOOKING THE SYMBOL ON THE BOX: ≋ ≙ LOW PASS; ≋ ≙ BAND PASS; ≋ ≙ HIGH PASS).
THAT **HAS TO REMOVE OUTBAND NOISE**.
THESE SIGNALS COULD BE AMPLIFIED BY A **LOW NOISE AMPLIFIER** BUT THERE'S NO NEED TO DESCRIBE THIS STEP.

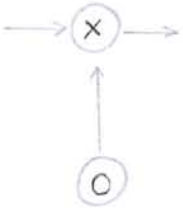


FIG. B1.7: multiplier (UP) and local oscillator (down)

THE DEVICE IN FIG B1.7 (UP) IS A **MULTIPLIER**: IT MULTIPLY TWO SIGNALS; IN THIS CASE THEY ARE:
- THE FILTERED (AND AMPLIFIED) INPUT SIGNAL, OF FREQUENCY f_{in}
- THE SIGNAL PRODUCT BY A LOCAL OSCILLATOR (FIG B1.7 DOWN), OF FREQUENCY f_{LO}.

THE LOCAL OSCILLATOR PRODUCES A STABLE-FREQUENCY SIGNAL WITH LOW PHASE NOISE AND ENOUGH OUTPUT POWER. IT CAN BE REALIZED WITH A CRISTAL OSCILLATOR.

THE BEHAVIOUR OF THE MULTIPLIER CAN BE DESCRIBED AS IN FIG B1.8 AND USING THE WERNER'S FORMULAE:

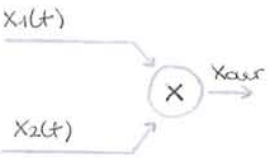


FIG B1.8 Multiplier

$$\begin{cases} x_1(t) = x(t)\cdot \text{sen}(2\pi f_{in} t) \\ \text{OR} \\ x_1(t) = x(t)\cos(2\pi f_{in} t) \end{cases} \qquad \begin{cases} x_2(t) = \text{sen}(2\pi f_{LO} t) \\ \text{OR} \\ x_2(t) = \cos(2\pi f_{LO} t) \end{cases}$$

$$\text{sen}(f_{in})\,\text{sen}(f_{LO}) = \frac{1}{2}\left[\cos(f_{in}-f_{LO}) - \cos(f_{in}+f_{LO})\right];$$

$$\Rightarrow \quad \text{sen}(f_{in})\cos(f_{LO}) = \frac{1}{2}\left[\text{sen}(f_{in}+f_{LO}) + \text{sen}(f_{in}-f_{LO})\right];$$

$$\cos(f_{in})\cos(f_{LO}) = \frac{1}{2}\left[\cos(f_{in}+f_{LO}) + \cos(f_{in}-f_{LO})\right]$$

SO THE OUTPUT OF THE MULTIPLIER IS COMPOSED OF TWO TERMS: ONE WITH FREQUENCY $f_{in}+f_{LO}$ AND ONE WITH FREQUENCY $f_{in}-f_{LO}$. ALL THESE TERMS ARE MULTIPLIED FOR X(t) WHICH IS THE BASE-BAND SIGNAL.
SO THE X(t) SPECTRUM IS TRANSLATED.
USUALLY WE'RE INTERESTED ONLY IN THE SIGNAL HAVING THE DIFFERENCE FREQUENCY $(f_{in}-f_{LO}) = f_{IF}$.
THIS HETERODYNE TECNIQUE ALLOWS TO MODIFY THE VALUE OF f_{IF} ACCORDING TO THE RADIO FREQUENCY SIGNAL, JUST CHANGING THE FREQUENCY OF THE LOCAL OSCILLATOR.

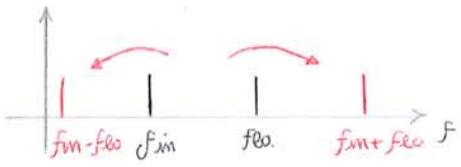


FIG B1.8 Frequency content of multiplier's output

SO:
- f_{in} DEPENDS BY THE INPUT SIGNAL (UNPREDICTABLE)
- f_{IF} IS A FIXED FREQUENCY (TO FILTER)
- f_{LO} CHANGES ACCORDING TO HAVE $f_{IF} = f_{in} - f_{LO}$.

SINCE f_{in} IS FIXED, WE CAN FILTER IT USING A FILTER WHOSE CHARACTERISTICS ARE FIXED! **THERE'S NO NEED TO REALIZE VARIABLE FILTERS.**

② ANOTHER SOLUTION IS BASED ON THE IDEA OF USING A MATHEMATICAL TRICK TO REMOVE f_{im}; IT REQUIRES PHASE SHIFTERS INSTEAD OF FILTERS IN ORDER TO APPLY THE I/Q PROCESSING.

NOTE: I/Q PROCESSING MEANS "IN-PHASE AND QUADRATURE" MODULATION. IF WE HAVE A REAL SIGNAL $x(t)$, WE CALL:

$x(t)\cos(2\pi f_c t)$ => "IN PHASE" COMPONENT
$x(t)\sin(2\pi f_c t)$ => "QUADRATURE" COMPONENT

SO WHAT IS THE IDEA:

- WE HAVE AN INPUT SIGNAL WHOSE "USEFUL" COMPONENT IS AT A FREQUENCY f_{im}, WHILE THE "UNWANTED" COMPONENT IS AT A FREQUENCY f_{IM}.
- WE WANT TO TRANSLATE f_{im} TO $f_{IF} = f_{im} - f_{LO}$ AND AT THE SAME TIME TO REMOVE THE COMPONENT AT $f = f_{IM} - f_{LO}$.

SUPPONING THAT BOTH INPUT SIGNALS AND OSCILLATOR'S OUTPUT SIGNAL ARE SINUSOIDS (NOTHING CHANGES IF WE CONSIDER A COSINUSOID) WE HAVE THAT, ACCORDING TO THE BLOCK DIAGRAM IN FIG B1.13:

sine (quadr.)

$$[\sin(f_{im}) + \sin(f_{IM})]\sin(f_{LO}) = \sin(f_{im})\sin(f_{LO}) + \sin(f_{IM})\sin(f_{LO}) =$$

APPLYING THE WERNER'S FORMULA ⑧:

$$= \frac{1}{2}[\cos(f_{im} - f_{LO}) - \cos(f_{im} + f_{LO})] + \frac{1}{2}[\cos(f_{IM} - f_{LO}) - \cos(f_{IM} + f_{LO})]$$

cos (phase)

$$[\cos(f_{im}) + \cos(f_{IM})]\cos(f_{LO}) = \cos(f_{im})\cos(f_{LO}) + \cos(f_{IM})\cos(f_{LO}) =$$ (same ⑧)

$$= \frac{1}{2}[\cos(f_{im} + f_{LO}) + \cos(f_{im} - f_{LO})] + \frac{1}{2}[\cos(f_{IM} + f_{LO}) + \cos(f_{IM} - f_{LO})]$$

IF WE SUM THESE EXPRESSIONS, WE OBTAIN:

$$\underbrace{\cos(f_{im} - f_{LO}) + \cos(f_{IM} - f_{LO})}_{\text{ONLY DIFFERENCE TERM!}}$$

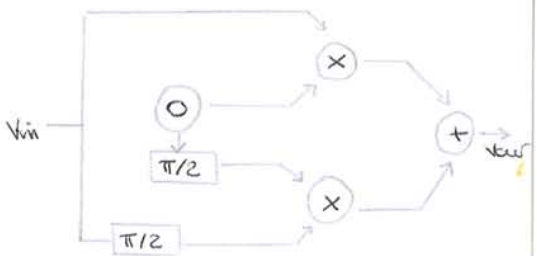


FIG B1.13 I/Q mixer

THIS CIRCUIT WAS USED MANY YEARS AGO; NOWADAYS ICs HAVE TAKEN OVER BECAUSE OF THE POSSIBILITY TO MATCH THE TWO PHASE SHIFTERS USING EXTERNAL CIRCUITS, IN AN EASIER AND LESS EXPENSIVE WAY. IN ORDER TO ENSURE THE CORRECT BEHAVIOUR OF THIS CIRCUIT, IN FACT, THE TWO PHASE SHIFTER MUST BE PERFECTLY MATCHED AND IT REQUIRES HIGH COSTS.

AN ALTERNATIVE SOLUTION IS SHOWN IN FIG. B1.14 AND IT'S CALLED "HARTLEY REJECTION MIXER". THIS TIME, THE IDEA IS OF SEPARETING I/Q PROCESSING (IN ORDER TO RESOLVE THE PROBLEM OF MATCHING) AND TO FILTER THE UNWANTED SIDEBAND COMPONENTS. IN THIS WAY WE CAN ALSO SEPARATE PHASE AND QUADRATURE INFORMATIONS TO MAKE THEM AVAILABLE FOR OTHER APPLICATIONS.

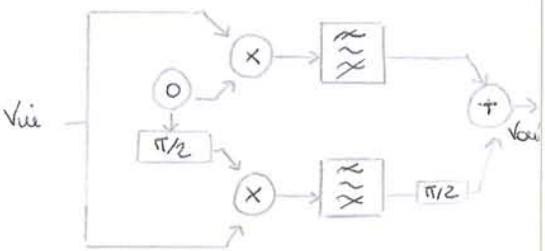


FIG B1.14 Separating I/Q processing

FIRST OF ALL, WE'VE TO CLEARLY UNDERSTAND WHAT IS THE BEST PLACE TO POSITION THE A/D CONVERTER AND WHY.

- 1ST OPTION: A/D AFTER THE DEMODULATOR

FIG B1.17: 1ST option

THIS IS NOT A GOOD IDEA BECAUSE APPLYING ERROR CORRETION, ENCRYPTING AND SO ON, ON AN ANALOG SIGNAL IS COMPLEX AND EXPENSIVE BECAUSE OF THE SIGNAL DEGRADATION DUE TO NOISE.

- 2ST OPTION: A/D BEFORE THE DEMODULATOR

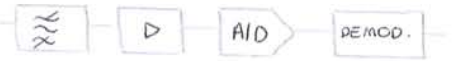


FIG B1.18: 2ST option

THIS IS A GOOD IDEA BECAUSE DIGITAL DEMODULATION TECNIQUES ARE MORE ACCURATE THAN ANALOG ONES, BESIDES ERRORS CORRECTIONS ARE EASIER TO APPLY. IN THIS CASE THE A/D WILL OPERATE IN IF BAND, SO AN HIGHER SAMPLING RATE IS REQUIRED.

- 3ST OPTION: A/D BEFORE THE I/F FILTER

FIG B1.19 3ST option

IN THIS CASE THE DIGITAL PROCESSOR MUST CARRY OUT ALSO DIGITAL FILTERING FUNCTIONS. DIGITAL FILTERS ARE EASIER TO BUILD AND MODIFY THAN ANALOG ONES, SO THIS COULD BE A GOOD IDEA. THE PROBLEM IS THAT THIS CONFIGURATION REQUIRES MORE COMPUTATIONAL POWER THAN THE PREVIOUS ONES AND IT MEANS $P_d \uparrow\uparrow$.

SO THE BEST OPTION IS THE 2ND ONE.

AN A/D CONVERTER IS BASED ON 3 STEPS:

- SAMPLING
- QUANTIZATION (THE REAL CONVERSION)
- CODING

SAMPLING CONVERTS A CONTINUOUS TIME-DOMAIN SIGNAL TO A DISCRETE TIME-DOMAIN SIGNAL. IT CAN BE MADE BY MULTIPLYING THE SIGNAL BY A TRAIN OF PULSES OF PERIOD T_c.

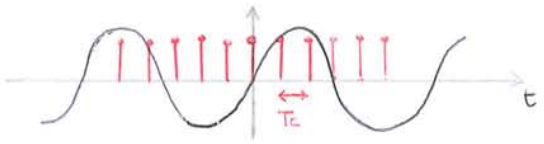


FIG B1.20 Sampling in time domain

SINCE SAMPLING IN THE TIME DOMAIN CORRESPONDS TO A REPLICATION IN THE FREQUENCY DOMAIN, TO AVOID THE OVERLAP OF THE REPLICAS (AND HENCE THE DISTORSION OF THE INFORMATIONS THEY CARRY), THE SAMPLING FREQUENCY MUST VERIFY THE NYQUIST SAMPLING CRITERIA:

$$f_c \geq 2B$$

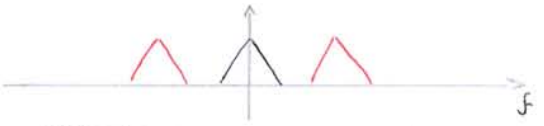


FIG B1.21 Sampling in f-domain when $f_c \geq 2B$

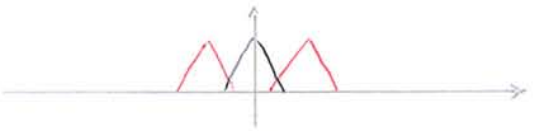


FIG B1.22 Sampling in f-domain when $f_c < 2B$

WHERE B IS THE BANDWIDTH OF THE SIGNAL. IN THIS HYPOTHESIS, THE SIGNAL CAN BE FILTERED WITH A LOW PASS FILTER AND RECONSTRUCTED IN ORDER TO PREVENT REPLICAS OF NOISE AND INTERFERENCES. AN ANTI-ALIASING FILTER CAN BE USED BEFORE OF SAMPLING.

FIG B1.23 Sampling in f-domain when there is noise.

THE PROBLEM IS THAT A RF SIGNAL HAS A VERY NARROW BAND AND A VERY HIGH FREQUENCY, SO IT'S DIFFICULT TO ISOLATE AND SAMPLING THEM. WE NEED PARTICULAR TECNIQUES.

FIG B1.28 Variable gain amplifier

IN THE END, WE'LL GIVE A LOOK TO SOME FULLY DIGITAL ARCHITECTURES SUCH AS THE SDR (SOFTWARE DESIGNED RADIO) IN FIG B1.29, WHERE AN HETERODYNE ARCHITECTURE AND A DIRECT SAMPLING STRUCTURE ARE SHOWN. EVERY COMPONENT, INCLUDING THE LOCAL OSCILLATOR, IS DIGITAL.

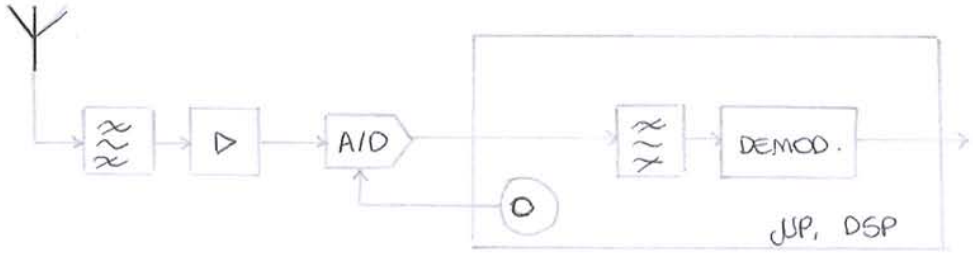


FIG B1.29 SDR (Software Designed Radio)

IN FIG B1.30, THE DIRECT SAMPLING DIGITAL I/Q PROCESSING STRUCTURE IMPLEMENTED IN THE SDR IS SHOWN. THERE ARE NO MIXER AND NO DOWN CONVERTER: IMAGE CANCELLATION IS ACHIEVED BY I/Q PROCESSING. IT CAN BE APPLIED ALSO WHEN WE HAVE A ZERO - f_{IF}.

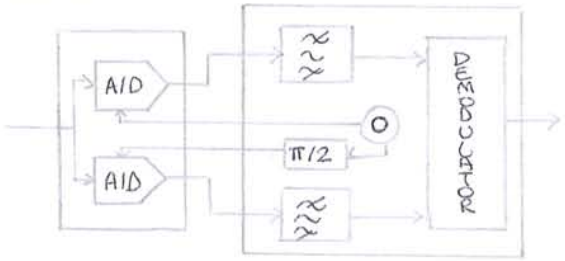


FIG B1.30 Direct sampling I/Q in SDR

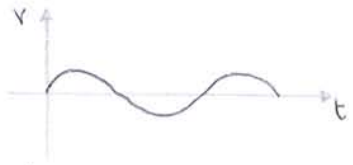
WE WROTE SO MUCH ABOUT RECEIVERS, BUT NOTHING ABOUT TRANSMITTERS. THAT'S WHY, HOW ANTICIPATED AT THE VERY BEGINNING, THE ARCHITECTURES OF TRASMITTERS ARE EQUALS TO THE ONES WE DESCRIBED FOR RECEIVERS, LESS THAN AMPLIFIERS. IN RECEIVERS WE USE LOW NOISE AMPLIFIERS, WHILE IN TRANSMITTER WE USE POWER AMPLIFIER IN ORDER TO HAVE A BETTER TRANSMISSION OF THE SIGNAL.

LESSON: 7 AND 8
DATE: 19-03-16 AND 21-03-16
PROF: D. DEL CORSO

B.2: AMPLIFIERS NONLINEARITY

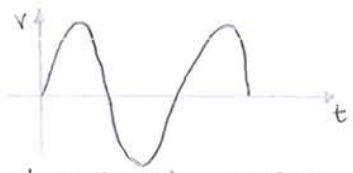
IN LESSON A3 WE ANALYZED BJT AMPLIFIERS IN THE HYPOTHESIS OF SMALL INPUT SIGNAL; WE SAW THAT, IN THIS APPROXIMATION, THE RELATION BETWEEN I AND O IS LINEAR, SO WE CAN USE A SIMPLIFIED MODEL TO ANALYZE THE AMPLIFIER BEHAVIOUR.

SO, IF FOR EXAMPLE WE PUT AS INPUT A SINUSOID WHOSE PICK VALUE IS "SMALL", WE OBTAIN AS OUTPUT A SINUSOID HAVING THE SAME FREQUENCY AND AN HIGHER AMPLITUDE, ACCORDING TO THE VOLTAGE GAIN.
THE FREQUENCY CONTENT OF THE OUTPUT SHOWS ONLY THE FUNDAMENTAL HARMONIC: THERE ARE NO DISTORSIONS



$V_{in} = V \cdot \sin(2\pi f_0 t)$
$V \ll V_t$

FIG B2.1 Input



$V_{out} = (A_V \cdot V)\sin(2\pi f_0 t)$
$A_V \cdot V < V_g$ (SUPPLY VOLTAGE)

FIG B2.2 Output

FIG B2.3 frequency content

NOW WE WANT TO ANALYZE WHAT APPENS WHEN WE PUT AS I A SIGNAL WHOSE AMPLITUDE IS NOT "SMALL": THE NONLINEARITY EFFECTS. CLEARLY WE CAN'T USE LINEAR MODELS, BUT WE CAN USE THE EBERS-MOLL MODEL, WHOSE EQUATIONS ARE VALID FOR ANY TYPE OF SIGNAL. WE'LL REFER TO BJT AMPLIFIERS BUT SIMILAR CONSIDERATIONS COULD BE DONE FOR MOS AMPLIFIERS. THE CHOICE IS DUE TO THE FACT THAT MOS I/O CHARACTERISTIC IS MORE COMPLEX AND CAN BE BETTER STUDIED USING NUMERICAL CALCULATORS.

AS USUAL, CONSIDER A COMMON-EMITTER CONFIGURATION.
THE FIRST STEP OF THE ANALYSIS IS BIASING, BUT NOTHING CHANGES COMPARED TO WHAT WE SEE IN LESSON A3, STEP ①.

EVERY TYPE OF BIAS CIRCUIT CAN BE REDUCED TO THE ONE SHOWN IN FIG B2.4 DOING AN APPROPRIATE CHOICE ON I_E AND V_E. WE CAN NOTE THAT THERE'S NO FEEDBACK RESISTANCE WHILE THERE IS A CAPACITOR CE, WHOSE FUNCTION IS TO KEEP THE E. TO GROUND FOR THE SIGNAL; PLUS THERE ARE TWO SUPPLY VOLTAGES, ONE POSITIVE AND ONE NEGATIVE.

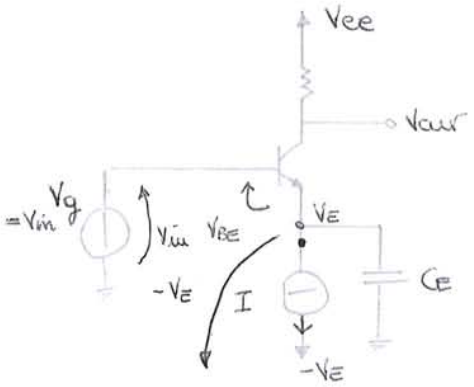


FIG B2.4 Reference circuit

IN THE FOLLOWING, WE'LL USE A CONVENTION:

- v_A => MAGNITUDE WHICH CHANGES INSTANT BY INSTANT
  - ↓ CAPITAL SUBSCRIPT
  - SMALL LETTER
- V_A => DC MAGNITUDE
  - CAPITAL LETTER AND SUBSCRIPT
- v_ω => AC MAGNITUDE
  - SMALL LETTER AND SUBSCRIPT

SO WE CAN WRITE $v_A = V_A + v_\omega(t)$.

WE HAVE TO NOTE THAT THE DC CURRENT I DEPENDS ON V_{in} THROUGH X. SO IF WE CHANGE V_{in} WE CHANGE I AND WE CHANGE V_E TOO!

V_E IS NOT REALLY FIXED, BUT HAS A LOGARITHMIC DEPENDENCE BY X:

$$I_{DC} = I_S\, e^{\frac{V_E}{V_t}} \cdot I_0(x) \Rightarrow V_E = V_t \cdot \ln\left(\frac{I}{I_S\, I_0(x)}\right)$$

SO V_E IS A VARIABLE DC VOLTAGE.

IN THE FOLLOWING, WE CAN SEE HOW i_c VARIES VS. INPUT SIGNAL VARIATIONS AND $I_m(x)/I_0(x)$ SWIPPING.

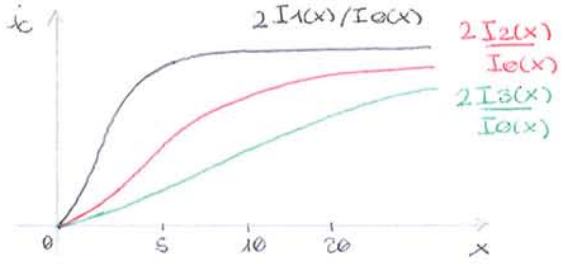


FIG B2.5 i_c VS. x, $I_m(x)/I_0(x)$ SWIPPING

x	$2\cdot\frac{I_1(x)}{I_0(x)}$	$2\cdot\frac{I_2(x)}{I_0(x)}$	$2\cdot\frac{I_3(x)}{I_0(x)}$	$2\cdot\frac{I_4(x)}{I_0(x)}$
0.0	0.0000	0.0000	0.0000	0.0000
0.1	0.0999	0.0024	0.0000	0.024
0.5	0.4850	0.0600	0.0050	0.124
1.0	0.8928	0.2144	0.0350	0.240
2.0	1.3955	0.6045	0.1866	0.433
3.0	1.6200	0.9400	0.3933	0.568
5.0	1.7868	1.2853	0.7585	0.719
7.0	1.8511	1.4711	1.0104	0.795
10.0	1.8872	1.6206	1.2490	0.854
14.0	1.9272	1.7247	1.4344	0.895
200	1.9493	1.8051	1.5883	0.926

IF WE ZOOM ON THE FIG. B2.5, WE CAN SEE THAT FOR VERY LOW SIGNAL LEVELS ($x \ll 1$), THE CURVE IS ALMOST LINEAR SO THE APPROXIMATION WE USE IN A3 WAS VALID.

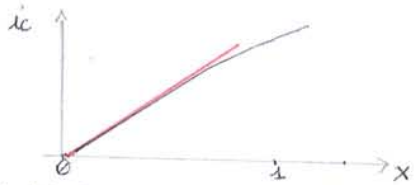


FIG B2.6 ZOOM ON B2.5

LET'S SEE HOW TO EXPRESS THE OUTPUT AND THE VOLTAGE GAIN.

$$V_{out} = -R_C I_C = -R_C \cdot I\left(1 + 2\sum_{M=1}^{+\infty}\frac{I_M(x)}{I_0(x)}\cdot\cos(2\pi M f_0 t)\right)$$

$$V_{in} = V_{IN}\cos(2\pi f_0 t) = \frac{V_{IN}\cdot V_t}{V_t}\cos(2\pi f_0 t) = x\cdot V_t\cos(2\pi f_0 t)$$

($\frac{V_{IN}}{V_t} = x$)

SO IF WE REFER TO THE FUNDAMENTAL HARMONIC:

$$A_V = \frac{V_{out}}{V_{in}} = -\frac{R_C \cdot I\, 2\frac{I_1(x)}{I_0(x)}\cos(2\pi f_0 t)}{x\, V_t \cos(2\pi f_0 t)} = -\frac{g_m}{x}\cdot\frac{2\,I_1(x)}{I_0(x)}\cdot R_C$$

(g_m)

WE RENAME:

$$G_M(x) = \frac{g_m}{x}\cdot\frac{2\,I_1(x)}{I_0(x)} \Rightarrow$$ LARGE SIGNAL TRANSCONDUCTANCE

NOTE THAT G_M DEPENDS ON X BUT ALSO ON g_m! SO WE CAN USE THIS MODEL ONLY AFTER HAVING DETERMINATED THE BIAS POINT!!

WE CAN NOTE THAT WHEN $x \to 0$, $I_M(x) \to x/2$ SO $G_M \to g_m$, IT MEANS THAT THE LINEAR CASE IS A SPECIAL CASE OF THE NONLINEAR CASE.

A WAY TO COMPENSATE THE GAIN COMPRESSION IS THE PREDISTORTION: IF WE ARE ABLE TO MEASURE THE LOSS OF POWER, WE CAN INTRODUCE ANOTHER DEVICE WHICH BALANCES THE COMPRESSION, AS SHOWN IN FIG B3.6:

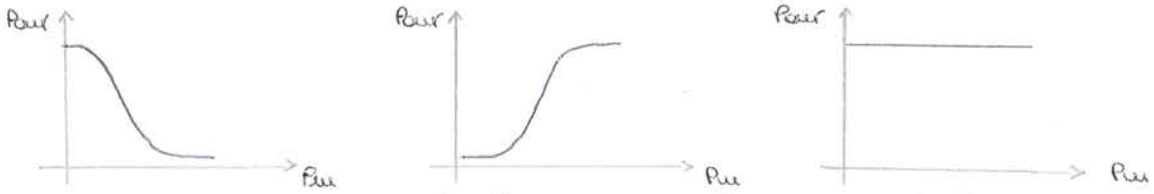


FIG B3.6 Gain compression's balance using predistortion

WE CAN STABILIZE THE GAIN USING THE CIRCUIT IN FIG B3.7, WHERE A NEGATIVE FEEDBACK ON THE EMITTER HAS BEEN INTRODUCED.
IN THIS WAY THE INPUT SIGNAL IS PARTIONATED AMONG V_{BE} AND R_E AND WE CAN USE R_E TO STABILIZE THE GAIN.
IF WE WRITE

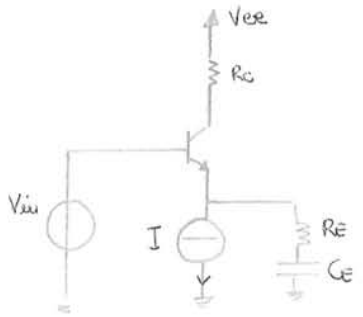


FIG B3.7 Emitter negative feedback

$$V_{BE} = V_{in} - \underbrace{R_E i}_{V_E} = \frac{V_{in}}{1 + G_m(x') \cdot R_E}$$

WHERE x' IS DEFINED BY AN EQUATION WITHOUT CLOSED FORM SOLUTION ⊛

$$x' = \frac{x}{1 + G_m(x') R_E}$$

SO THE OUTPUT IS

$$v_{out} = \frac{G_m(x')}{1 + G_m(x') \cdot R_E} R_C V_{in}$$

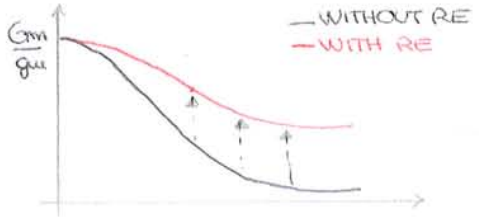


FIG B3.8 Gain compression with and without R_E

HOWEVER, WE CAN TAKE ADVANTAGES OF THE GAIN COMPRESSION TO REALIZE SEVERAL DEVICES SUCH AS:

- COMPRESSOR
- MIXER
- VGA (VARIABLE GAIN AMPLIFIER)
- OSCILLATOR
- LNA (LOW NOISE AMPLIFIER)

↓

BECAUSE WHEN THE INPUT SIGNAL IS SMALL, THE NONLINEARITY PRODUCES A VERY HIGH GAIN.

⊛ HOW CAN WE SOLVE THIS EQUATION? RECURSIVELY.

1. CONSIDER $x' = x$ AND SUBSTITUTE IT IN $G_m(x)$; WATCH HOW MUCH THE EQUATION IS WRONG
2. CHANGE VALUE AND TRY TO OBTAIN SOMETHING BETTER
3. CONTINUE UNTIL THE TERMS HAVE A SMALL DIFFERENCE!

HOW CAN WE EXACTLY OBTAIN THESE EFFECTS?
ACCORDING TO FIG. B3.11, Z IS A FUNCTION OF ω.
EVERY CONTRIBUTE FOR EVERY HARMONIC IS MULTIPLIED FOR THE CONTRIBUTE OF IMPEDANCE IN HARMONIC'S FREQUENCY, OBTAINING:

$$V_{out} = I \cdot |Z_c(\omega)| \frac{2 I_K(x)}{I_0(x)} \cdot \cos(\omega t)$$

THERE'S A CONTRIBUTE TO THE NON LINEAR BEHAVIOUR DEPENDING BY Z_c. WE'VE TO QUANTIFY THIS TERM IN ORDER TO MULTIPLY IT TO THE PREVIOUS TERM..
WE CAN EVALUATE

$$X = \left| \frac{Z(\omega_0)}{Z(K\omega_0)} \right| = Q \left| K - \frac{1}{K} \right|$$

AND SUM IT TO THE BESSEL FUNCTION CONTRIBUTE.

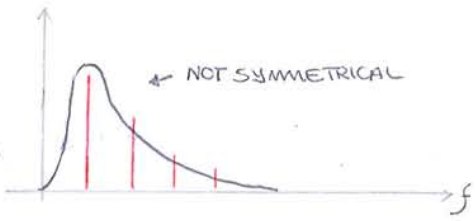


FIG B3.14 Tuned circuit effect

WE COULD KEEP THIS TYPE OF DISTORSION TO REALIZE
- FREQUENCY MULTIPLIERS
- TUNED AMPLIFIERS

INTERMODULATION

THE INTERMODULATION IS AN EFFECT DUE TO THE APPLICATION OF TWO INPUT SIGNALS OR, THAT'S EQUIVALENT, A SIGNAL WITH TWO TONES WHICH ARE VERY CLOSED.
IN ORDER TO BETTER UNDERSTAND THIS EFFECT, WE CAN WRITE THE OUTPUT SIGNAL AS A POWER SERIES EXPRESSION, OR RATHER AS THE SUM OF A LINEAR TERM, A QUADRATIC TERM, A CUBIC TERM AND SO ON:

$$V_{out} = A \cdot V_{in} + B \cdot V_{in}^2 + C V_{in}^3 + \dots$$

IF WE CONSIDER $V_{in} = V_{IN} \cdot \cos(2\pi f_0 t)$, WE HAVE:

$$V_{out} = A \cdot \cos(2\pi f_0 t) + B \cos(2\pi (2 f_0) t) + C \cos(2\pi (3 f_0) t) + \dots$$

NOW LET'S CONSIDER $V_{in} = V_{IN1} \cos(2\pi f_1 t) + V_{IN2} \cos(2\pi f_2 t)$:

$$V_{out} = A[\cos(2\pi f_1 t) + \cos(2\pi f_2 t)] + B[\cos^2(2\pi f_1 t) + \cos^2(2\pi f_2 t) + 2 \underline{\cos(2\pi f_1 t)\cos(2\pi f_2 t)}] + C[\cos^3(2\pi f_1 t) + \cos^3(2\pi f_2 t) + \underline{3\cos^2(2\pi f_1 t)\cos(2\pi f_2 t)} + \underline{3\cos^2(2\pi f_2 t)\cos(2\pi f_1 t)}] + \dots$$

IF WE APPLY THE WERNER'S FORMULAE TO THE UNDERLINED TERMS, WE'LL NOTE THAT THE OUTPUT CONTAINS TONES AT FREQUENCIES:

- $f_1 \pm f_2$
- $2f_1 \pm f_2$
- $2f_2 \pm f_1$

THESE COMPONENTS ARE IN BAND AND CAN'T BE FILTERED EASILY, ESPECIALLY THE TERM WHICH IS RELEATED TO THE III ARMONIC!

THIS SPURIOUS SIGNALS ALTER THE INFORMATION CONTENT, SO WE'VE TO REMOVE THEM USING NARROW BAND FILTERS.

FIG B3.15 Intermodulation effect

EXAMPLE: TRANSISTOR

- CONSIDER A BJT (OR MOS) AMPLIFIER.
  THE FIRST THING TO DO IS TO RECOGNIZE THE CONFIGURATION. (COMMON-EMITTER? COMMON GATE?)

▶ BIAS ANALYSIS

USUALLY WE HAVE TO BIAS THE CIRCUIT BY USING A GIVEN STRUCTURE AND BY FOLLOWING SOME SPECIFICATIONS.
IN MOST OF THE CASE, WE'VE A CIRCUIT LIKE THE ONE IN FIG. ① AND, SINCE THE COLLECTOR RESISTANCE DOESN'T INVOLVES INTO THE BIAS, WE CAN USE THE EQUIVALENT CIRCUIT IN FIG ② WHERE:

FIG. ① BIAS

$$R_B = R_{B1} \,//\, R_{B2}$$
$$V_{BB} = V(R_{B2}) = V_{AL} \cdot \frac{R_{B2}}{R_{B1}+R_{B2}}$$

IF WE HAVE β_{FE} VERY LARGE, WE CAN ASSUME:

$$I_E \approx I_C \longrightarrow I_B = \frac{I_C}{\beta_{FE}}$$

SO WE CAN WRITE THE KIRCHOFF RULE:

$$V_{BB} = V(R_B) + V_{BE} + V(R_E) = R_B \cdot I_B + 0.6V + R_E I_C$$

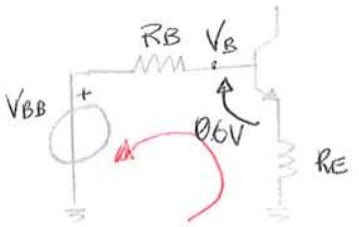


FIG ② EQUIVALENT CIRCUIT

▶ WE CAN EVALUATE THE OUTPUT DYNAMIC WITH OR WITHOUT LOAD AND CHOSE R_C IN ORDER TO MAKE IT SYMMETRIC.

$$\Delta V_{out}\big|_{no\ load\ pp} = V_{CC} - V_{CE_{sat}} - R_E I_E$$

$$R_C = \frac{1}{2}\left(\Delta V_{out}\big|_{no\ load}\right) \cdot \frac{1}{I_C}$$

THIS IS A GOOD CHOICE! REMEMBER THAT WE MUST KEEP $V_{CE} \gg V_{CE\,sat}$ SO OTHER GOOD CHOICES CAN BE:
$V_C = V_{AL}/2$
$V_C = V_{AL}/3$

$$\Delta V_{out}\big|_{load\ pp} = \left(\Delta V_{out}\big|_{no\ load}\right) \frac{R_{load}}{R_C + R_{load}}$$

IF WE'VE AN INPUT SIGNAL THAT PROVIDES AN OUTPUT THAT'S OVER THE DYNAMIC RANGE, WE'VE DISTORSION. (TRUNCATION)

BANDWIDTH

CONSIDER THE MOST USED CONFIGURATION IN FIG. (4) ; WE'VE THAT:

$$\omega = \frac{1}{\tau} \longrightarrow f = \frac{1}{2\pi\tau}$$

WHERE

$$\tau_i = C_i \cdot R_{eqi}$$

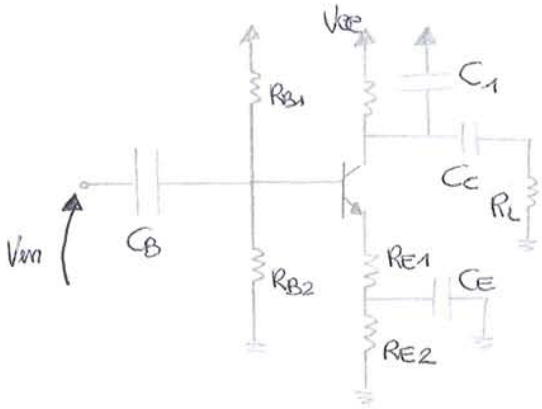


FIG (4) COMMON-EMITTER CONF.

IN THE FOLLOWING WE PROVIDE SOME EQUIVALENT RESISTANCES ASSOCIATED TO SOME OF THE CAPACITORS.

$$R_{eq_B} = R_{B1} \,//\, R_{B2} \,//\, (R_{IE} + R_{E1} \cdot R_{FE})$$ → USUALLY C_B IS RESPONSABLE OF THE LF LIMIT

$$R_{eq_1} = R_C \,//\, R_L$$ → USUALLY C_1 IS RESPONSABLE OF THE HF LIMIT AND MAKES A LOW-PASS CELL

$$R_{eq_C} = R_C + R_L$$ → USUALLY C_C DOESN'T MODIFY THE HF LIMIT

ABOUT C_E :

IT HAS NOT A QUALITATIVE INFLUENCE IN THE MASK BECAUSE IT INTRODUCES POLES ONLY AT LOWER FREQUENCIES THAN f_2 BUT HIGHER THAN f_1, AS SHOWN IN FIG. (5)

FIG (5) EFFECT OF C_E ON THE MASK

▶ IF IT'S ASKED TO REPLACE RC WITH A LC CIRCUIT OR TO PUT IT IN // WITH RC, THE FIRST THING TO DO IS TO EVALUATE:

$$Q = \frac{X}{\left|K - \frac{1}{K}\right|}$$

WHERE X IS THE ATTENUATION AND WE'LL TO EXPRESS IT IN NATURAL

K IS THE HARMONIC OF INTEREST

IT'S USUALLY GIVEN IN dB AS THE SEPARATION BETWEEN FUNDAMENTAL AND HARMONIC → WE'LL TO MODIFY THIS VALUE ACCORDING TO THE RESULT OF THE PREVIOUS ANALISYS. OR RATHER:

$$X = X^{*}_{dB} - \left(\frac{I_2}{I_1}\right)_{dB}$$

THE TUNED CIRCUIT ON THE COLLECTOR DOESN'T MODIFY I_C (BIAS IS INDIPENDENT FROM THE LOAD ON THE COLLECTOR).

IT HAS HIGHEST IMPEDANCE AT $\omega_{Res.}$, THEREFORE THE VOLTAGE GAIN IS HIGHEST FOR THE III HARMONIC ($3\omega_i$), AND OTHER SPECTRAL COMPONENTS ARE ATTENUATED.

THE OUTPUT SPECTRUM INCLUDES A STRONG $3\omega_i$ COMPONENT.

THE CIRCUIT IS A FREQUENCY MULTIPLIER.

LESSON: 9 AND 10
DATE: 24-03-16 AND 26-03-16
PROF: D. DEL CORSO

B4 : SINE SIGNAL GENERATORS

SINE SIGNAL GENERATORS ARE PART OF OSCILLATORS : CIRCUITS THAT PRODUCE A REPETITIVE, OSCILLATING ELECTRONIC SIGNAL (A SINE WAVE OR A SQUARE WAVE). THEY CONVERT A DC CURRENT FROM A POWER SUPPLY TO AN ALTERNATING CURRENT SIGNAL, WHICH IS CHARACTERIZED BY THE FOLLOWING PARAMETERS:

$$v(t) = V \cdot \text{sen}(\omega t + \vartheta)$$

- V AMPLITUDE
- ω ANGULAR FREQUENCY $\rightarrow \omega = 2\pi f \rightarrow f = 1/T$
- ϑ PHASE

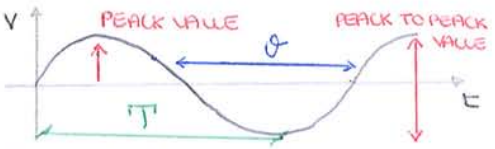


FIG B4.1 Sine wave

THE SIGNAL IS EFFECTED BY

- UTILE HARMONIC SPURIOUS
- PHASE NOISE

USUALLY, OSCILLATORS ARE CLASSIFIED ACCORDING TO THE RANGE OF FREQUENCIES OF THEIR OUTPUT SIGNALS.

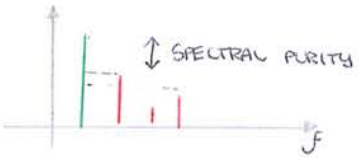


FIG B4.2 Spurious

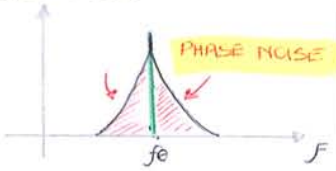
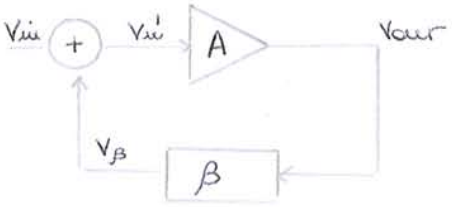


FIG B4.3 Phase noise

(1) THE MOST COMMON FORM OF OSCILLATOR IS AN ELECTRONIC AMPLIFIER (SUCH AS A TRANSISTOR OR AN OP AMP) CONNECTED IN A FEEDBACK LOOP WITH ITS OUTPUT FED BACK INTO ITS INPUT THROUGH A FREQUENCY SELECTIVE FILTER TO PROVIDE POSITIVE FEEDBACK (POSITIVE BECAUSE THE OUTPUT SIGNAL PRESERVS ITS POLARITY).
THE CONDITIONS IN WHICH THIS DEVICE WORKS AS AN OSCILLATOR CAN BE FOUND EASILY:



B4.4 oscillator block diagram

$$V_{out} = A \cdot V_{in}' = A \cdot (V_{in} + V_\beta) = A(V_{in} + \beta \cdot V_{out})$$

$$\Rightarrow V_{out} = \frac{A V_{in}}{1 - \beta A}$$

SO THE CLOSED LOOP TRANSFER FUNCTION IS:

$$A(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{A(s)}{1 + A(s)\beta(s)}$$

THE BEHAVIOUR OF THE DEVICE DEPENDS ON THE POSITIONS OF THE POLES IN THE COMPLEX PLANE OF $s = x + jy$:

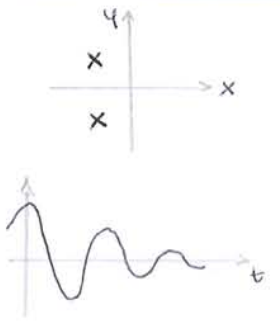


FIG B4.5 stability

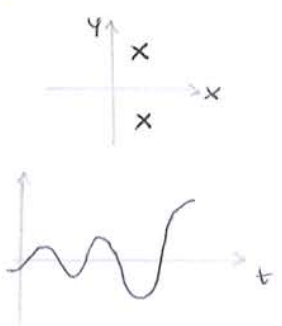


FIG B4.6 instability

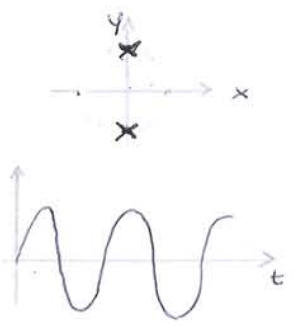


FIG B4.7 constant amplitude oscillations

① COLPITTS OSCILLATOR

THE β-BLOCK IS A CAPACITIVE VOLTAGE DIVIDER.

APPARENTLY, IT DOESN'T INTRODUCE FREQUENCY SHIFT, BECAUSE:

$$V_R = V_{out} \cdot \frac{C_1}{C_1 + C_2}$$

BUT ACTUALLY IT DOES. BECAUSE FROM THE EMITTER WE SEE AN EQUIVALENT RESISTANCE EQUAL TO $1/g_m$ AND g_m DEPENDS ON FREQUENCY!

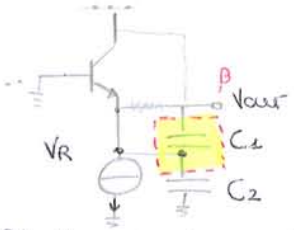


FIG B4.11 Colpitts oscillator

② HARTLEY OSCILLATOR

THE β-BLOCK IS AN INDUCTIVE VOLTAGE DIVIDER, WITH A FEEDBACK LOOP.
WE CAN DO THE SAME OBSERVATIONS DONE FOR COLPITTS' ONE.

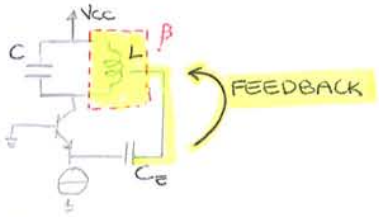


FIG B4.12 Hartley oscillator

③ MEISSNER OSCILLATOR

THE β-BLOCK IS A TRANSFORMER;
WE CAN REVERSE THE PHASE.

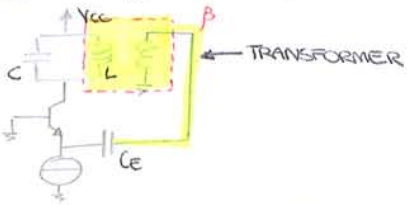
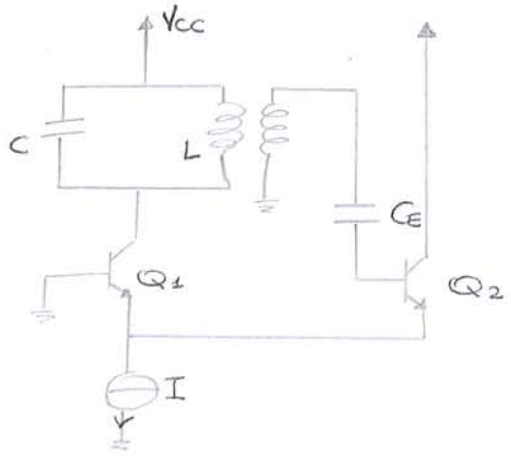


FIG B4.13 Meissner oscillator

IN ORDER TO REDUCE THE LOAD ON THE FEEDBACK, WE CAN USE ANOTHER TRANSISTOR AS EMITTER FOLLOWER, OBTAINING A DIFFERENTIAL STADIUM:



(ISOLATES LC GROUP FROM Q1 EMITTER)

FIG B4.14 Differential configuration

THE NIC CAN BE USED ALSO TO TRANSFORM AN INDUCTANCE INTO A CAPACITANCE AND VICEVERSA.
THE OP AMP CAN BE SUBSTITUDE BY DISCRETE COMPONENTS.
AN EXAMPLE OF "-gm" CIRCUIT IS SHOWN IN FIG B4.18. WE CAN SEE THAT THERE ARE NO OP AMP BUT ONLY TRANSISTORS, IN ORDER TO OBTAIN HIGH FREQUENCY OSCILLATIONS. THE FIRST STADIUM IS A DRAIN COMMON, SO IT PROVIDES TO THE INERTION OF THE OUTPUT.

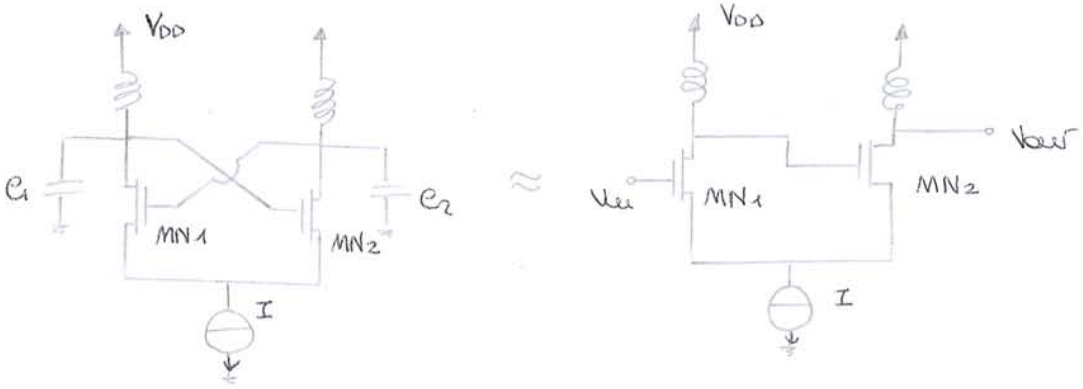


FIG B4.18 Differential circuit for NIT.

THE BENEFITS OF DIFFERENTIAL STRUCTURE ARE LESS NOISE, NO EVEN HARMONICS,

(3) A PARTICULAR TYPE OF OSCILLATOR IS THE QUARTZ OSCILLATOR DESCRIBED IN LESSON B1 AS A PIEZOELECTRIC MATERIAL WHICH, UNDER MECHANICAL PRESSURE, GENERATES ELECTRICAL SIGNALS.
THE QUARTZ OSCILLATOR IS CHARACTERIZED BY A VERY HIGH QUALITY FACTOR

$$Q \triangleq \frac{\text{AVERAGED ENERGY STORED}}{\text{ENERGY LOSS}}$$

IN GENERAL Q IS A FUNCTION OF ω_0 AND R

- SERIES RESONATORS
  - IF R ↓ → LOSS ↓ → Q ↑
  - IF ω_0 ↓ → Q ↑
- PARALLEL RESONATORS
  - IF R ↑ → LOSS ↓ → Q ↑
  - IF ω_0 → Q ↑

NOTE: HOW IF WE WANT TO CHANGE THE RESONANT FREQUENCY?
THE RESONANT FREQUENCY IS $\omega_0 = 1/\sqrt{LC}$, SO WE HAVE TO CHANGE L OR C IN THE WAYS DESCRIBED IN LESSON B1.
A CIRCUIT WHICH IS VERY USED TO VARY THE RESONANT FREQUENCY IS SHOWN IN FIG B4.19 AND IT'S BASED ON A VARICAP DIODE.
THE VARICAP DIODE IS A TUNING DIODE WHOSE CAPACITANCE VARIES AS A FUNCTION OF THE VOLTAGE APPLIED ACROSS ITS TERMINALS.

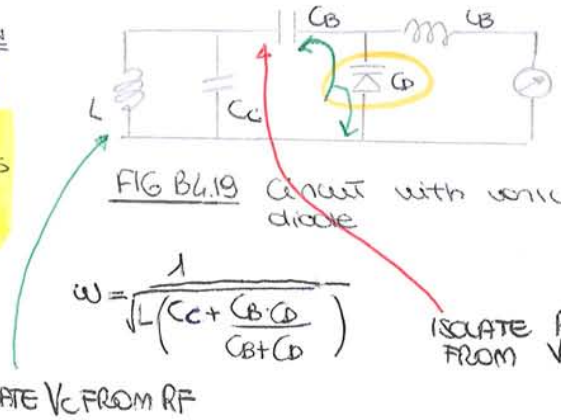


FIG B4.19 Circuit with varicap diode

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MULTIPLIERS

- ANALYSIS

3 OPTIONS:

- MATHEMATICAL TRICK
- TRANSCONDUCTANCE MULTIPLIERS
  - SINGLE QUARTER
  - BALANCED
  - DOUBLE BALANCED
  - DIFFERENTIAL COUPLE
- DIODES
  - SINGLE
  - BRIDGE

NOW LET'S SEE HOW CAN WE REALIZE MULTIPLIERS. THERE ARE 3 IDEAS:

1. USING NON LINEAR CIRCUITS
2. USING TRANSISTORS
3. USING DIODES

1) MULTIPLIERS WITH NONLINEAR CIRCUITS

THE IDEA IS THE FOLLOWING ONE: IF WE CONSIDER A NON LINEAR CIRCUIT, SUCH AS AN AMPLIFIER, GIVEN TWO INPUT SIGNALS WE'LL HAVE NONLINEAR TERMS. AMONG THEM, WE CAN ISOLATE THE USEFUL ONE, FOR EXAMPLE

$$(V_1+V_2)^2 = V_1^2 + V_2^2 + 2V_1V_2$$

WE CAN EASILY REALIZE THIS TYPE OF CIRCUIT USING TRANSISTORS (OPAMP ARE TOO LINEAR). HOWEVER, THIS CIRCUIT HAS THE BIG DISADVANTAGE OF REQUIRING AN ACURATE FILTERING SYSTEM, AND WE KNOW THAT THEY'RE EXPENSIVE AND DIFFICULT TO REALIZE.

2) MULTIPLIERS WITH TRANSCONDUCTANCE CIRCUITS

THE IDEA IS THE FOLLOWING ONE: IF WE DEAL WITH SMALL SIGNALS, WE CAN ANALYZE TRANSISTOR AMPLIFIERS USING LINEAR MODELS.
WE KNOW THAT FOR A COMMON EMITTER CONFIGURATION THE VOLTAGE GAIN IS PROPORTIONAL TO g_m:

$$A_V \propto g_m ; \quad g_m = \frac{I_C^*}{V_t}$$

g_m DEPENDS ON I_C^* WHICH IS FIXED BY THE BIAS ANALYSIS, BUT IF WE CHANGE I_C^*, g_m CHANGES AND A_V CHANGES.
THE IDEA IS TO INTRODUCE A SECOND TRANSISTOR WHOSE INPUT VOLTAGE CONTROLS I_C^* AND SO g_m. IN THIS WAY

$$V_{out} = A_V \cdot V_{in} \propto \underbrace{g_m(V_2)}_{\text{FUNCTION OF } V_2} \cdot V_1$$

(PRODUCT)

THAT'S WHY THIS TYPE OF CIRCUIT IS CALLED "TRANSCONDUCTANCE": BECAUSE IT WORKS BY CONTROLLING g_m!

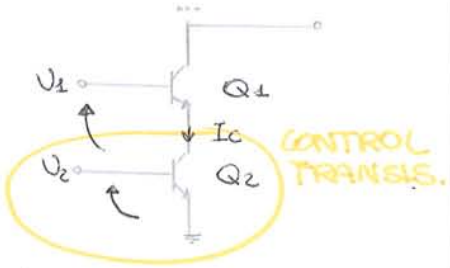

FIG B5.6 Transconductance circuit (idea)

WHAT ARE THE LIMITS OF THIS CONFIGURATION?

- IT WORKS ONLY WHEN WE DEAL WITH SMALL SIGNALS
- IF WE WANT TO APPLY A SINE INPUT, WE HAVE TO PAY ATTENCTION: WE NEED THAT IT HAS AN OFFSET IN ORDER TO NOT TURN OFF THE TRANSISTOR.

↓

THIS PROBLEM CAN BE SOLVED USING MORE COMPLEX CONFIGURATIONS.

WHAT ARE THE ADVANTAGES OF THIS CONFIGURATION?

- WE WORK IN LINEARITY, SO WE DON'T HAVE DISTORSIONS.

↓

IF WE WANT, WE CAN USE A TUNED CIRCUIT AS LOAD TO FILTER NOISE AND OTHER DISTORSIONS.

THE LIMIT OF TRANSCONDUCTANCE CIRCUITS IS THE SMALL DYNAMIC RANGE DUE TO THE APPROXIMATION OF LINEARITY. IN ORDER TO IMPROVE THE RANGE, WE CAN USE FEEDBACK, IN PARTICULAR A NEGATIVE FEEDBACK ON THE EMITTER TERMINAL.
IN THIS WAY, THE GAIN DECREAS AND THE STABILITY IS INCREASED.
IF WE ADD TWO R_E ON EMITTERS, AS IN FIG B5.10,
WE HAVE THAT:

$$I' - I'' \cong \frac{V_{in2}}{2R_E}$$

IF $R_E' = R_E''$. WE NEED TO MATCH THESE RESISTANCES IN ORDER TO AVOID AN UNBALANCE OF V_{EE}'S AND COMMON MODE ISSUES.
SINCE MATCHING RESISTANCES IS QUITE DIFFICULT, WE CAN USE THE CIRCUIT IN FIG B5.11 WITH AN UNIQUE RESISTANCE. IN THIS WAY, WE HAVE

$$I' - I'' = \frac{V_{in}}{R_X}$$

FOR BOTH CASES, WE NEED TO CONVERT VOLTAGE TO CURRENT USING MATCHED CURRENT SOURCES WHICH CAN BE REALIZED ONLY IN IC.

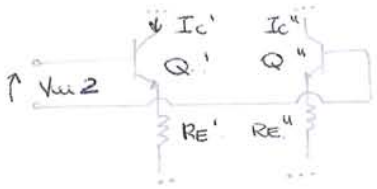

FIG B5.10 2-resistances negative feedback

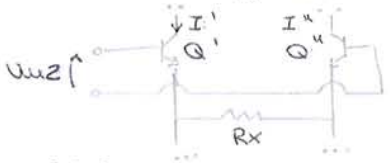

FIG B5.11 Single resistance negative feedback

THIS CIRCUIT CAN REPLACE THE DIFFERENTIAL STADIUM FOR V_{in2}, BUT NOT THE ONE FOR V_{in1}, BECAUSE THE PRINCIPLE OF A MULTIPLIER IS USING THE RELATION $\Delta I_C(I_E, V_A)$. AN IDEA CAN BE THE FOLLOWING ONE: WE USE THE CIRCUIT IN FIG B5.11 ALSO FOR "V_{in1}" AND COMPENSATE THE UNBALANCE USING ANOTHER DIFFERENTIAL STADIUM THAT IS PILOTED BY THE FIRST ONE.
WE OBTAIN A VERY COMPLEX CIRCUIT THAT CAN BE SCHEMATIZED AS IN FIG. B5.12

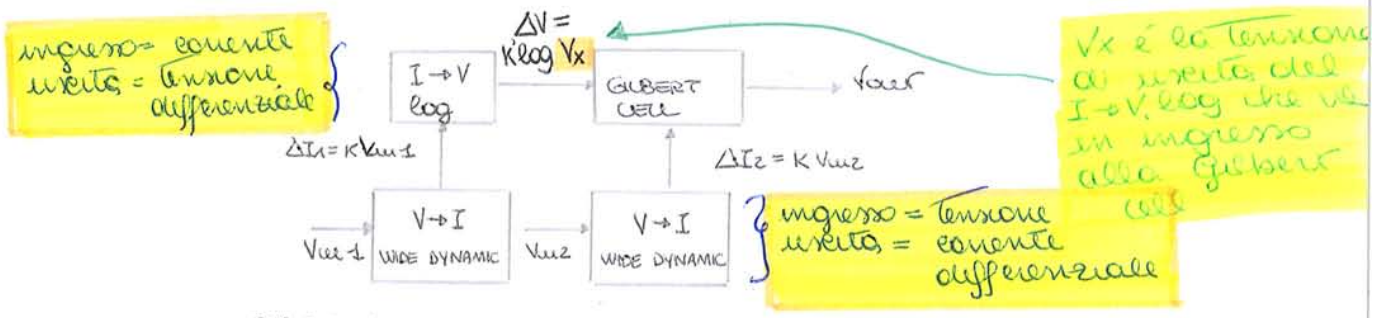

FIG B5.12 Wide-range multiplier: block diagram

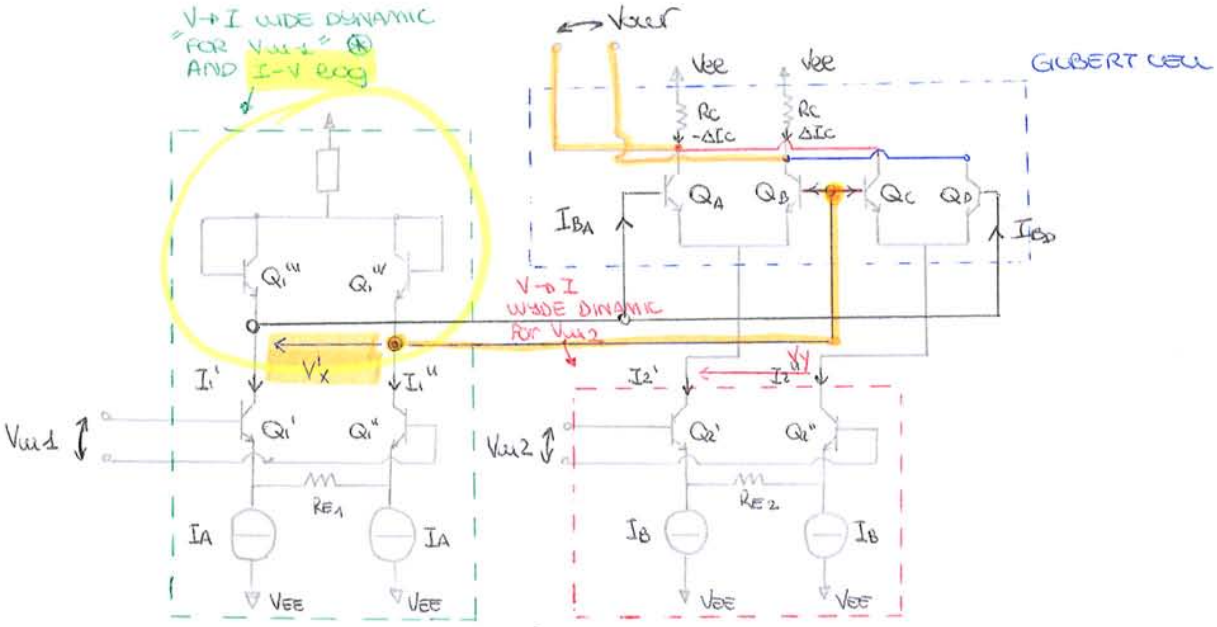

FIG B5.13 Wide range multiplier

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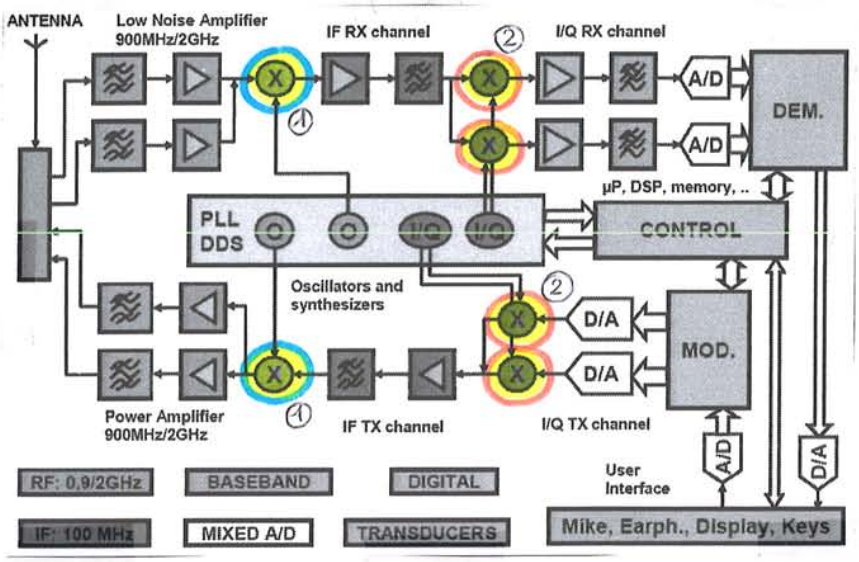
MULTIPLIERS IN A RF ARCHITECTURE



① RF MIXERS FOR THE FIRST CONVERSION

② I/Q MIXERS FOR THE SECOND CONVERSION

PLUS WE CAN FIND MULTIPLIERS IN GPS SYSTEMS:

- IN THE RECEIVER ⇒
  1) IMAGE - REJECTION MIXER
  2) OTHER MIXERS
  3) PLL AS MULTIPLIER
  4) AMPLIFIER AS MULTIPLIER

LESSON: 12
DATE: 28-03-14
PROF: D. DEL CORSO

B.6 : NON LINEAR CIRCUITS (LOGARITHMIC AMPLIFIERS)

WE'RE GOING TO STUDY HOW TO REALIZE A CIRCUIT WHOSE TRANSFER FUNCTION HAS A PARTICULAR NON LINEAR SHAPE. FOR EXAMPLE A LOGARITHMIC SHAPE. WE CHOSE TO STUDY THIS TYPE OF AMPLIFIER BECAUSE USUALLY LOGARITHMIC AMPLIFIERS ARE USED TO MEASURE POWER (THINK OF THE dB SCALE).
CLEARLY, WE'LL NEVER DESIGN A CIRCUIT WHOSE TRANSFER FUNCTION IS PERFECTLY IDENTICAL TO THE DESIRED ONE; WE'LL ALWAYS HAVE SOME APPROXIMATIONS. THERE ARE 2 WAYS WE CAN USE TO OBTAIN A NON LINEAR BEHAVIOUR (AND SO A LOGARITHMIC ONE):

- USE A CONTINUOUS APPROXIMATION: THE ACTUAL TRANSFER FUNCTION IS CONTINUOUS AND COULD BE OBTAINED USING SIMPLE CIRCUITS; HOWEVER, IT'S USUALLY MORE APPROXIMATED (LOG→PARABOLIC; PARABOLIC→LINEAR)
- USE A PIECEWICE APPROXIMATION: THE ACTUAL TRANSFER FUNCTION IS COMPOSED BY MANY LINES WHOSE SLOPES DEPEND ON THE INPUT VOLTAGE AMPLITUDE

IN ORDER TO OBTAIN A LOGARITHMIC TRANSFER FUNCTION, THE PIECEWICE APPROXIMATION IS THE BEST ONE; HOWEVER IT REQUIRES VERY COMPLEX CIRCUITS, SO WE'LL USE A WORST APPROXIMATION (THE CONTINUOUS ONE) BUT SIMPLER CIRCUITS. IN THE END WE'LL SEE HOW TO SIMULATE A LOGARITHMIC TRANSFER FUNCTION USING PIECEWICE APPROXIMATION BUT WITHOUT ENTERING INTO DETAILS.

WE WANT TO REALIZE A CIRCUIT WHOSE OUTPUT IS RELEATED WITH THE INPUT BY A LOGARITHMIC RELATION:

$$V_{out} = \log(V_{in}) \quad \text{IDEAL}$$

IN REALITY, WE'LL HAVE A RELATION LIKE:

$$V_{out} = K_1 \cdot \log\left(K_2 \cdot (V_{in} + K_4)\right) + K_3 \quad \text{REAL}$$

WHERE TERMS K_1, K_2, K_3, K_4 DENOTE ERRORS AND DISTORSIONS.
IF WE PLOT THE LOGARITHMIC RELATION IN A SEMI-LOGARITHMIC AXES, AS IN FIG B6.2, WE CAN BETTER ANALYZE THESE TERMS AND THEIR EFFECTS.

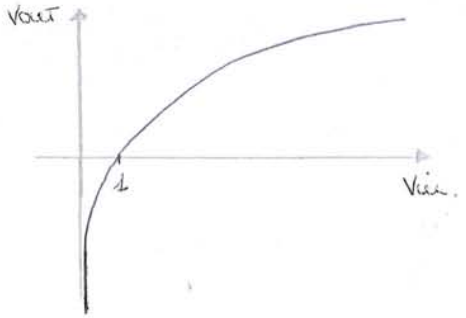


FIG B6.1 Logarithmic function

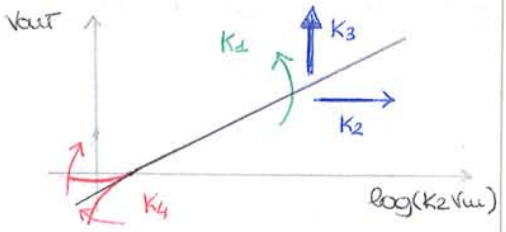


FIG B6.2 Logarithmic function in a semi-logarithmic scale

- K_1 MODIFIES THE SLOPE OF THE TRANSFER FUNCTION, SO IT GENERATES A ROTATION.
- K_2 AND K_3 HAS THE SAME EFFECT BUT IN TWO DIFFERENT DIRECTIONS, RESPECTIVELY; THEY GENERATE AN HORIZONTAL AND A VERTICAL SHIFT OF THE CHARACTERISTIC.
- K_4 CAUSES NON LINEARITY FOR LOW VALUES OF V_{in}: IT'S CRITICAL BECAUSE A SHIFT OF FEW MILLIVOLT CAN CHANGE THE BEHAVIOUR OF THE CIRCUIT WHEN WE DEAL WITH SMALL SIGNALS.

ALL THESE EFFECTS CAN BE SYNTHESIZED IN THE FOLLOWING SCHEME:

FIG B6.3 Block diagram of a logarithmic amplifier

THE FIRST STEP TO REALIZE A LOGARITHMIC AMPLIFIER IS TO FIND SOMETHING THAT CAN REALIZE A LOGARITHMIC RELATION, CLEARLY, THE SIMPLEST DEVICE IS A DIODE.

$$I = I_S\, e^{\frac{V}{V_t}} \quad \longleftrightarrow \quad V = V_t \cdot \ln\left(\frac{I}{I_S}\right)$$

IN REALITY WE NEED TO CONSIDER A FACTOR η:

$$V = \eta V_t \ln\left(\frac{I}{I_S}\right) = (\eta \ln(I) - \eta \ln(I_S))\, V_t$$

WHICH IS

- $\eta = 1 \Rightarrow$ FOR TRANSISTORS
- $\eta = 2 \Rightarrow$ FOR DIODES

SO, WE HAVE THAT IF V IS THE OUTPUT, I IS THE INPUT.
IN ORDER TO FORCE A CURRENT IN A DIODE, WE CAN PUT IT IN AN OP-AMP FEEDBACK CONFIGURATION, AS HINTED IN THE DIGRESSION ABOUT OP AMP:

WE HAVE:

$$I_R = I_D$$

SO:

$$\frac{V_{in}}{R} = I_S\, e^{\frac{V_d}{V_t}}$$

BUT $V_d = -V_{out}$, SO:

$$\frac{V_{in}}{R} = I_S\, e^{\frac{-V_{out}}{V_t}}$$

$$\rightarrow V_{out} = -V_t \ln\left(\frac{V_{in}}{R}\,\frac{1}{I_S}\right) = -V_t \ln(V_{in}) + V_t \ln(R \cdot I_S)$$

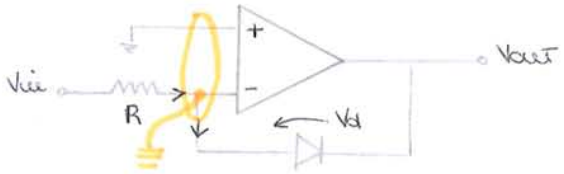


FIG B6.4 OPAMP with negative diode feedback

TAKING INTO ACCOUNT OF THE FACTOR η:

$$V_{out} = -\eta V_t \ln(V_{in}) + \eta V_t \cdot \ln(R \cdot I_S)$$

IF WE COMPARE THIS EXPRESSION WITH THE IDEAL ONE (*), WE HAVE

$$K_1 = -\eta V_t$$

$$K_2 = \frac{1}{R \cdot I_S}$$

K_3 AND K_4 ARE DUE TO NOISE AND DISTORSIONS AND CAN'T BE TAKEN INTO ACCOUNT IN THE ANALYSIS BY HAND.

WE HAVE TO NOTICE THAT K_1 AND K_2 HAVE A STRONG DEPENDENCE ON TEMPERATURE (DUE TO η, V_t AND I_S).
WE CAN REDUCE THIS EFFECT AND GIVE STABILITY TO THE CIRCUIT INTRODUCING A MORE COMPLEX CIRCUIT WITH A FEEDBACK NETWORK COMPOSED OF TWO RESISTANCES WHICH VARIE WITH TEMPERATURE (FIG B6.5) AND, EVEN BETTER, INSERTING A RESISTANCE BETWEEN THE OUTPUT OF THE OP AMP AND THE TWO EMITTERS IN ORDER TO REDUCE THE LOOP GAIN (FIG B6.6).
NOTE THAT THE FIRST JUNCTION (WHICH CAN BE A DIODE OR A BJT) IS INTRODUCED TO MAKE THE GAIN INDIPENDENT BY η, WHILE THE SECOND ONE TO ACT ON V_T AND I_S

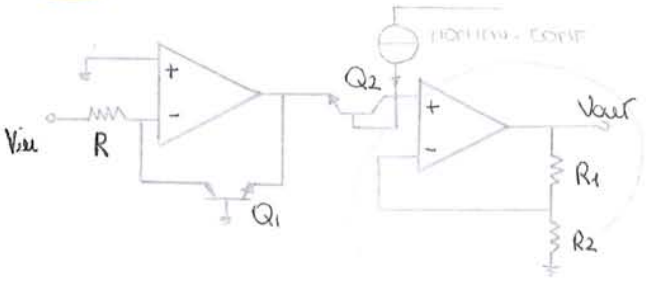


FIG B6.5 Basic Circuit for log. ampl.

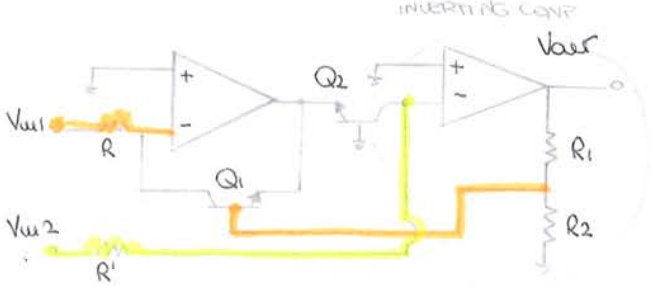


FIG B6.6 Ratiometric log. ampl.

IF WE WANT TO OBTAIN A BIPOLAR CHARACTERISTIC, IN ORDER TO DEAL WITH BOTH POSITIVE AND NEGATIVE INPUT VOLTAGES, WE HAVE TO ADD ANOTHER DIODE, AS SHOWN IN FIG B6.9.

IN THIS WAY, WE ALWAYS HAVE A DIODE ON. HOWEVER, SINCE THERE IS AN UNUSUAL BEHAVIOUR OF THE CHARACTERISTIC AROUND THE ORIGIN, WE CAN'T SAY THAT IT'S A LOGARITHMIC AMPLIFIER. HOWEVER, THIS CIRCUIT CAN WORK AS A COMPRESSION AMPLIFIER: IT COMPRESSES HIGH SIGNALS IN ORDER TO AVOID SATURATION OR DE-COMPRESSES LOW SIGNALS WHICH HAS BEEN TREATED BY THE DIGITAL PART OF THE RECEIVER.

IF $V_{in} > 0 \Rightarrow D_2$ ON $\Rightarrow V_{out} < 0$
IF $V_{in} < 0 \Rightarrow D_1$ ON $\Rightarrow V_{out} > 0$

↓

INVERTENT!

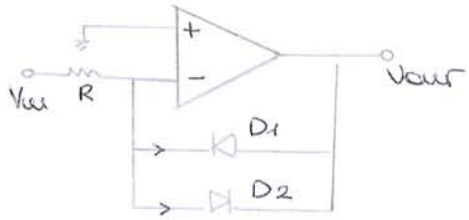


FIG B6.9 Bipolar logarithmic amplifier

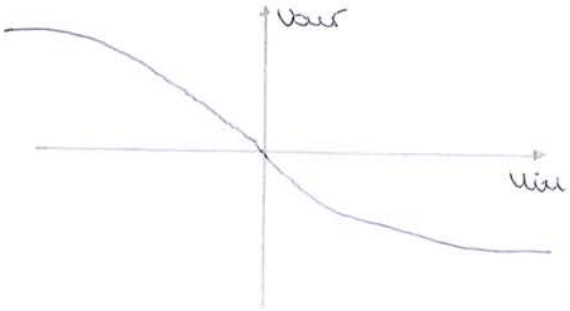
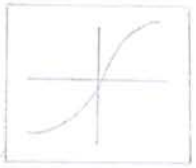


FIG B6.10 Bipolar logarithmic amplifier transfer function

NOTE: THE GENERAL SYMBOL FOR A COMPRESSOR IS SHOWN IN FIG B6.11 AND THE CURVE IS DIFFERENT FROM THE ONE IN FIG B6.10 BECAUSE IT'S REFERRED TO AN INVERTENT CONFIGURATION.



B6.11 Compressor symbol

LESSON: 12
DATE: 28-03-16
PROF: D. DEL CORSO

C1: PLL LINEAR ANALYSIS

A PLL (PHASE LOCK LOOP) IS A CONTROL SYSTEM THAT GENERATES AN OUTPUT SIGNAL WHOSE PHASE IS RELEATED TO THE PHASE OF AN INPUT SIGNAL. PLUS, THIS OUTPUT SIGNAL IS A CLEAR SIGNAL WITH FEW NOISE, HIGH AMPLITUDE, NICE SHAPE, FEW DISTORSIONS: THAT'S WHY THE PLL CAN REALIZE MANY FUNCTIONS THANKS TO ITS STRUCTURE, THAT ESSENTIALLY CONSISTS IN A PHASE DETECTOR, A FILTER, A VOLTAGE CONTROL OSCILLATOR AND A FEEDBACK LOOP, AS SHOWN IN FIG C1.1.

USUALLY, PLLS ARE USED AS

- SYNCHRONIZER
- FILTER
- SYNTHESIZER
- DEMODULATOR

SO, THEY ARE EMPLOYED IN RADIO, TELECOMMUNICATIONS, COMPUTERS, MOBILE PHONES AND SO ON.

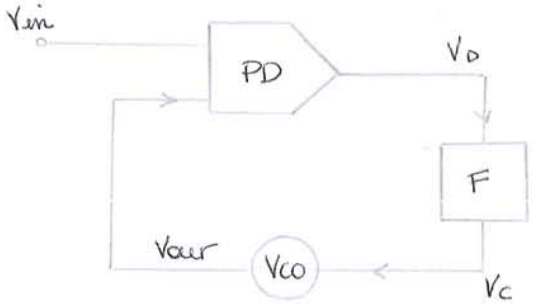


FIG C1.1 PLL block diagram

LET'S MAKE A PRELIMINARY ANALYSIS OF THE PLL BLOCK DIAGRAM IN ORDER TO UNDERSTAND THE BEHAVIOUR OF THE DEVICE; THEN WE'LL ANALYZE THE SINGLE DEVICES.

$$V_{in} = V_{in} \cdot \sin(\omega_i t + \underbrace{\vartheta_i}_{\text{PHASE}})$$

REMEMBER THAT THE ANGULAR FREQUENCY ω AND THE PHASE ARE RELEATED:

$$\Delta\omega = \frac{d\vartheta}{dt} \Rightarrow \Delta\omega = s\,\vartheta(s)$$

(LAPLACE DOMAIN)

PD IS A PHASE DETECTOR, A DEVICE THAT GENERATES A SIGNAL WHICH REPRESENTS THE DIFFERENCE IN PHASE BETWEEN THE TWO INPUT SIGNAL. IN THIS CASE, THE INPUT SIGNALS ARE V_{in} AND $-V_{out}$, THAT IS THE OUTPUT OF V_{CO}, THE VOLTAGE CONTROL OSCILLATOR. THE VCO IS A DEVICE WHOSE INPUT IS A DC VOLTAGE AND WHOSE OUTPUT IS A SIGNAL WHOSE FREQUENCY DEPENDS ON THE INPUT SIGNAL BY AN USUALLY NON LINEAR RELATION ($\Delta\omega = \omega(V_c)$)

IF WE CONSIDER

$$V_{out} = V_{out} \cos(\omega_{out} t + \vartheta_{out})$$

WE'LL HAVE THAT THE OUTPUT OF THE PD WILL BE SOMETHING LIKE:

$$V_D = F(\vartheta_{in} - \vartheta_{out}) = F(\vartheta_e)$$

WHERE WE DEFINE

$\vartheta_e \triangleq \vartheta_{in} - \vartheta_{out}$ => PHASE ERROR

F IS A GENERIC, NON LINEAR, FUNCTION

THIS SIGNAL IS FILTERED BY A FILTER THAT USUALLY IS A LOW PASS FILTER. THE OUTPUT SIGNAL IS A DC VOLTAGE WHICH ENTERS INTO THE VCO GIVING LIFE TO A FEEDBACK LOOP.

WHEN WE'VE

- $\omega_i \neq \omega_{out}$ => ϑ_e VARIABLE => NO LOCK
  THE SIGNAL MOVES ON THE DISPLAY OF THE SCOPE BECAUSE THERE IS A CONTINUOUS PHASE SHIFT: THE TRIGGER IS NOT ABLE TO SYNCHRONIZE ITSELF WITH THE SIGNAL
- $\omega_i = \omega_{out}$ => ϑ_e CONSTANT => LOCK
  THE PHASE DIFFERENCE BETWEEN THE TWO SIGNALS IS PRESENT BUT CONSTANT.
  THE OUTPUT SIGNAL IS CLEAR, WITH ANY DISTORSION AND FEW NOISE.

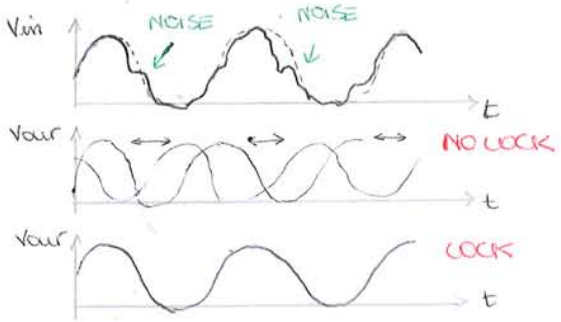


FIG C1.2 PLL behaviour

RC CELL

$$F(S) = \frac{1}{1+SRC} \quad (\text{I ORDER})$$

$$H(S) = K_0K_D \frac{1}{1+SRC} \cdot \frac{1}{S + K_0K_D \cdot \frac{1}{1+SRC}} =$$

$$= \frac{K_0K_D}{S^2RC + S + K_0K_D} \quad (\text{II ORDER}) \Rightarrow \text{LOW PASS FILTER}$$

THE ANDAMENT OF THE TRANSFER FUNCTION DEPENS ON:

$$\omega_N = \sqrt{\frac{K_0K_D}{RC}} \; ; \; \xi = \frac{1}{RC} \cdot \frac{1}{2\omega_N} = \frac{1}{2} \cdot \frac{1}{\sqrt{K_0K_DRC}}$$

$H(0) = 1$

APPARENTLY WE HAVE 4 DEGREES OF FREEDOM, BUT IN REALITY WE'VE ONLY 2: RC AND K_0K_D. IT MEANS THAT WE CAN'T CONTROL THE SYSTEM THAT IS VERY UNSTABLE.

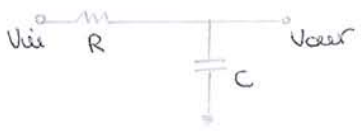


FIG C1.5 RC cell

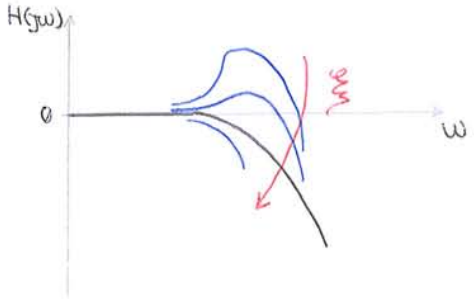


FIG C1.6 PLL Transfer Fuction with an RC cell filter

R-RC CELL

THIS CONFIGURATION IS MORE STABLE, IN FACT WE HAVE A ZERO--POLE COUPLE:

$$F(S) = \frac{SR_2C + 1}{S(R_1+R_2)C + 1} \quad (\text{I ORDER})$$

$$H(S) = K_0K_D \cdot \frac{(SR_2C+1)}{S(R_1+R_2)C+1} \cdot \frac{1}{S + \frac{K_0K_D[S(R_2+1)]}{S(R_1+R_2)C+1}} =$$

$$= \frac{K_0K_D S R_2C + K_0K_D}{S^2(R_1+R_2)C + S(1 + K_0K_DR_2C + K_0K_D)} \quad (\text{II ORDER})$$

$\Rightarrow$ LOW PASS FILTER

WE HAVE:

$$\omega_N = \sqrt{\frac{K_0K_D}{(R_1+R_2)C}} \; ; \; \xi = \frac{1}{2}\left(R_2C + \frac{1}{K_0K_D}\right)\sqrt{\frac{K_0K_D}{(R_1+R_2)C}} \; ; \; H(0) = 1$$

SO THE DEGREES OF FREEDOM ARE 3: K_0K_D, R_1+R_2, R_2.

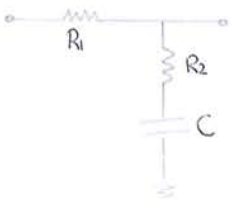


FIG C1.7 R-RC cell

ACTIVE RC CELL

THIS SOLUTION ALLOWS TO INCREASE THE NOMINAL GAIN, $H(0)$. THE OPAMP IS AN ACTIVE COMPONENT THANKS TO WHICH WE CAN EASILY MODIFY THE GAIN AND HAVE A WIDE FREQUENCY RANGE WITH A VERY SMALL PHASE ERROR IN THE INPUT LOOP. THIS CHOICE IS GOOD WHEN WE NEED A WIDE DYNAMIC.

IN FIG. C1.8, AN INFINITE-GAIN AMPLIFIER IS SHOWN. IT'S ESSENTIALLY AN INTEGRATOR AND ITS TRANSFER FUNCTION IS:

$$F(S) = -\frac{1}{SRC} \quad (\text{I ORDER})$$

$$H(S) = \frac{-K_0K_D}{S^2RC - K_0K_D} \quad (\text{II ORDER}) \Rightarrow \text{LOW PASS FILTER}$$

AS SEEN FOR THE RC CELL, THIS SOLUTION IS VERY UNSTABLE; WE'VE ONLY TWO DEGREES OF FREEDOM.

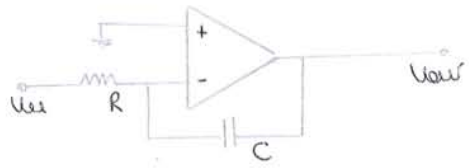


FIG C1.8 RC active cell

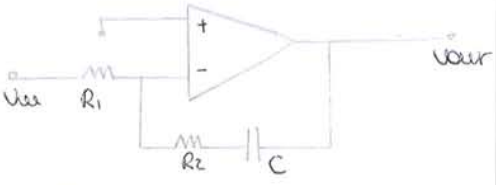


FIG C1.9 R-RC active cell

LESSON: 13
DATE: 31-03-16
PROF: D. DEL CORSO

STEADY STATE PHASE ERROR

WE'RE GOING TO ANALYZE THE STEADY STATE BEHAVIOUR OF THE SYSTEM AND, IN PARTICULAR, OF THE PHASE ERROR.
WE HAVE DEFINED THE PHASE ERROR AS

$$\vartheta_e = \vartheta_{in} - \vartheta_{out}$$

THE STEADY STATE PHASE ERROR IS THE VALUE OF ϑ_e WHEN THE SYSTEM IS IN THE STEADY STATE, SO THE TRANSIENT IS ENDED:

$$\vartheta_{eR} = \lim_{t \to \infty} \vartheta_e(t) = \lim_{s \to 0} s \cdot \vartheta_e(s)$$

(LAPLACE)

THIS ANAUYSIS IS VERY IMPORTANT BECAUSE IT ALLOWS US TO UNDERSTAND FOR WHAT TYPES OF INPUT SIGNAL THE SYSTEM LOCKS OR NOT, IN FACT WE KNOW THAT WE'LL LOCK WHEN

$$\vartheta_e = \text{costante}$$

THE BEHAVIOUR OF THE SYSTEM DEPENDS ALSO ON THE TYPE OF FILTER, SO WE'RE GOING TO ANALYZE ϑ_{er} FOR DIFFERENT TYPES OF:

- INPUT SIGNALS
  - PHASE STEP
  - PHASE RAMP
  - PARABOLIC PHASE
- FILTER
  - FINITE GAIN → $F(s) =$ costante
  - INFINITE GAIN → $F(s) \to \infty$ WHEN $s \to 0$

REMIND THAT

$$\vartheta_{er} = \lim_{s \to 0} s\vartheta_e(s) = \lim_{s \to 0} s \cdot \frac{s \cdot \vartheta_i(s)}{s + K_0 K_D F(s)} = \lim_{s \to 0} \frac{s^2 \vartheta_i(s)}{s + K_0 K_D F(s)}$$

PHASE STEP

A PHASE-STEP SIGNAL IS OF THE TYPE SHOWS IN FIG C1.13. IT CAN CHARACTERIZE A PSK (PHASE SHIFT KEYING) SIGNAL.

$$\vartheta_i = \frac{\Delta\vartheta_i}{s}$$

SO

$$\vartheta_{eR} = \lim_{s \to 0} \frac{s\Delta\vartheta_i}{s + K_0 K_D F(s)}$$

IF THE FILTER HAS FINITE GAIN:

$$\vartheta_{eR} = \lim_{s \to 0} \frac{\Delta\vartheta_i}{1 + \frac{K_0 K_D \cdot F(s)}{s}} = 0$$

($\frac{K_0 K_D \cdot F(s)}{s} \to \infty$)

IF THE FILTER HAS INFINITE GAIN:

$$\vartheta_{eR} = \lim_{s \to 0} \frac{s\Delta\vartheta_i}{s + K_0 K_D F(s)} = 0$$

($K_0 K_D F(s) \to \infty$)

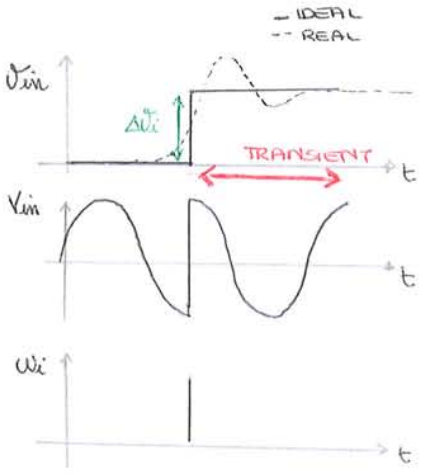
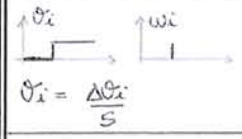
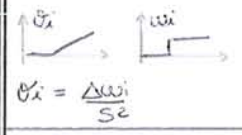
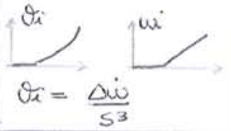


FIG C1.13 Phase-step signal

WE CAN PUT THESE RESULTS INTO A TABLE :

INPUT SIGNAL \ FILTER	FINITE GAIN $F(S)=\text{const.}$	INFINITE GAIN $F(S)\to\infty$, $S\to 0$
 $\vartheta_i = \frac{\Delta\vartheta_i}{S}$	$\vartheta_{er} = 0$	$\vartheta_{er} = 0$
 $\vartheta_i = \frac{\Delta\omega_i}{S^2}$	$\vartheta_{er} = \frac{\Delta\omega}{K_0 K_D F}$	$\vartheta_{er} = 0$
 $\vartheta_i = \frac{\Delta\dot{\omega}}{S^3}$	$\vartheta_{er} \to \infty$	$\vartheta_{er} = \frac{\Delta\dot{\omega}}{K_0 K_D}$

WE CAN CONCLUDE THIS ANALYSIS SAYING THAT THE LOCK IS POSSIBLE IN ALL CASES EXCEPT FOR ✱ BECAUSE THERE IS AN UNDETERMINATED RATIO.

CLEARLY WE HAVE TO TAKE INTO ACCOUNT THAT THIS ANALYSIS IS APPROXIMATED BECAUSE WE ASSUMED A LINEAR BEHAVIOUR OF THE PD AND OF THE VCO.

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IN ORDER TO REDUCE THE EFFECT OF K_D, WE MAY INTRODUCE A DYNAMIC RANGE COMPRESSION AT THE INPUT, FOR EXAMPLE A LOGARITHMIC AMPLIFIER.

ANOTHER IDEA IS TO REALIZE THE PD USING A DIFFERENT NON LINEAR CIRCUIT.

FIG C2.4 Range Compression at the input

WE WANT TO SHOW THAT ANALOG PDs CAN BE USED ALSO IF WE'VE AS INPUT A COUPLE OF SQUARE WAVES.

IF WE CONSIDER THE PRODUCT OF TWO GENERIC SQUARE WAVES AND LET IT PASS THROUGH A LOW PASS FILTER, WE OBTAIN ITS DC COMPONENT.

THE DC COMPONENT IS RELEATED WITH THE AREA OF THE SIGNAL WHICH IS RELEATED WITH THE PHASE; SO WE CAN WORK WITH SQUAREWAVES!

HOWEVER, ANALOG PDs ARE QUITE EXPENSIVE, SO THEY ARE NOT VERY USED.

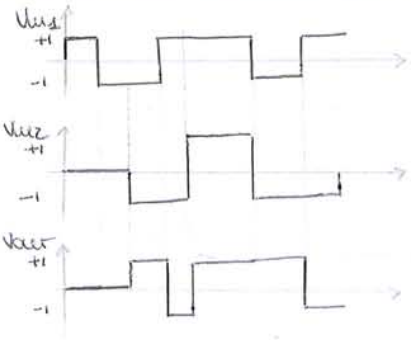

FIG C2.5 Product of two square waves

▶ DIGITAL PDs

IN ORDER TO STUDY DIGITAL PDs, WE'VE TO DEFINE THE PHASE SHIFT ALSO FOR DIGITAL SIGNALS: THESE SIGNALS ARE SIMILAR TO SQUARE WAVES BUT CAN ASSUME ONLY TWO VALUES CALLED UPPER STATE AND LOWER STATE.

IF WE CONSIDER PERIODIC SIGNALS OF PERIOD 'T' AND INDICATE WITH τ THE TIME INTERVAL IN WHICH THE SIGNAL IS IN THE UPPER STATE, WE CAN DEFINE:

$$\vartheta_e = \frac{\tau}{T} \cdot 2\pi$$

WHERE THE DENORMALIZATION IS INTRODUCED IN ORDER TO OBTAIN A DEFINITION SIMILAR TO THE OLD ONE.

EVEN THIS TIME WE CAN CONSIDER ONLY $\tau < T$, IN ORDER TO HAVE A RECOGNASEBLED PHASE SHIFT.

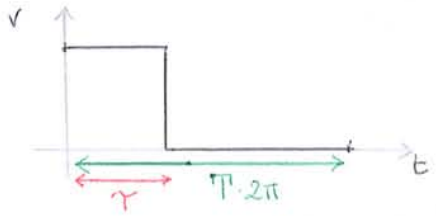

FIG C2.6 Digital Phase error

WE CAN REALIZE DIGITAL PDs USING 3 TECHNIQUES:

1) XOR
2) SR-FLIP FLOP
3) CHARGE PUMP

1) XOR PDs (PDs WORK WITH SQUAREWAVE)

THE SYMBOL, THE TRUTH TABLE AND THE BEHAVIOUR OF THE LOGIC GATE XOR (OR "EXCLUSIVE OR") ARE SHOWN IN THE FOLLOWING FIGURES:

FIG C2.7 XOR symbol

Vin1	Vin2	Vout
0	0	0
0	1	1
1	0	1
1	1	0

FIG C2.8 XOR truth Table

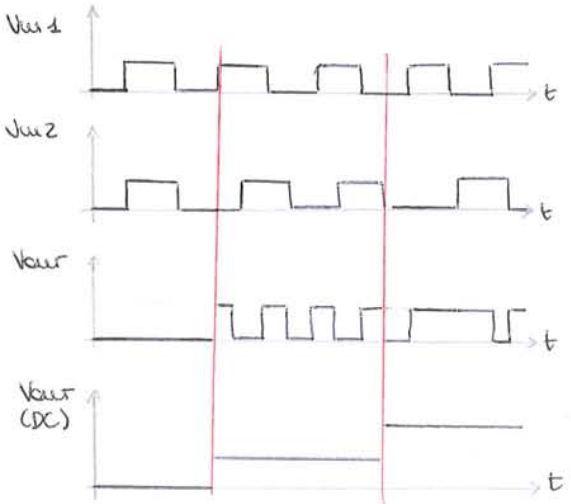

FIG C2.9 XOR behaviour

THE DC COMPONENT IS RELEATED TO THE AREA OF THE OUTPUT SIGNAL AND IT INCREASES WHEN THE PHASE SHIFT BETWEEN THE INPUT SIGNALS INCREASES.

$$K_D = \frac{V_S}{\pi}$$

IF WE CONSIDER SIGNALS WITH 50% DUTY CYCLE, OR RATHER SIGNALS WHOSE $\tau = T/2$, WE CAN SAY THAT:

- IF WE HAVE NO PHASE SHIFT, $V_{out} = 0$
- $V_{out\,DC}$ ↑ WHEN PHASE SHIFT ↑
- $V_{out\,DC}$ ↓ WHEN PHASE SHIFT ↓

THE OUTPUT IS MAXIMUM WHEN THE PHASE SHIFT IS MAXIMUM, SO EQUAL TO π.

THANKS TO THESE CONSIDERATION, WE OBTAIN THE GRAPH IN FIG C2.10.

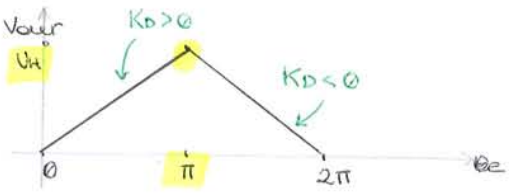

FIG C2.10 Symmetric Duty Cycle characteristic

WE CAN SAY THAT ALSO THIS TIME THERE IS A CHANGE IN POLARITY DUE TO K_D, BUT THIS TIME WE'VE A LINEAR CHARACTERISTIC SO WE CAN EVALUATE K_D!

IF WE CONSIDER THE POINT WHEN WE'VE $\theta_e = \pi$, $V_{out} = V_H$ THAT'S A PARAMETER DEPENDING BY THE TECNOLOGY OF THE XOR GATE. SO:

$$V_{out} = K_D \cdot \theta_e \Rightarrow K_D = \frac{V_{out}}{\theta_e} = \frac{V_H}{\pi}$$

IF WE CONSIDER SIGNALS WITH A DIFFERENT DUTY CYCLE, $\neq 50\%$, THE BEHAVIOUR OF THE PD DOESN'T CHANGE BUT IT CAN'T SENSE SOME θ_e CHANGES, SUCH AS VERY LOW AND VERY HIGH VALUES. IT CAUSES A REDUCTION OF THE USABLE CHARACTERISTIC.

A SOLUTION COULD BE TO DIVIDE THE SIGNALS BY TWO, IN THIS WAY ALSO K_D IS DIVIDED BY TWO ($K_D = V_H/2\pi$) AND WE DO NOT HAVE THIS PROBLEM ANYMORE.

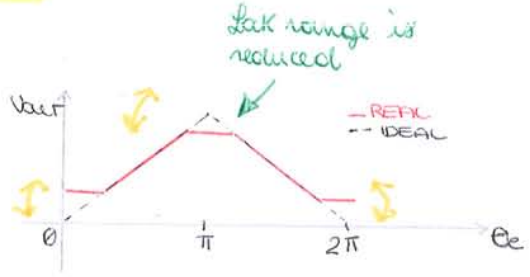

FIG C2.11 Asymmetric Duty cycle characteristic

2) S-R FLIP FLOP PDS (PDS WORK WITH PULSE)

THE BASIC STRUCTURE AND THE BEHAVIOUR OF A S-R FLIP FLOP ARE SHOWN IN THE FOLLOWING FIGURES:

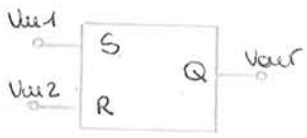

FIG C2.12 SR-symbol

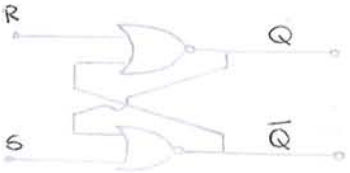

FIG C2.13 SR basic structure

S	R	Q	
0	0	0	→ HOLD STATE
0	1	0	→ RESET
1	0	1	→ SET
1	1	1	→ NOT ALLOWED

FIG C2.14 SR operation

REMEMBER THAT IF R AND S COMMUTES IN THE SAME INSTANT, WE CAN'T KNOW HOW THE SYSTEM WILL ACT BECAUSE IT'LL DEPEND ON THE STATE OF THE SYSTEM.

SINCE $V_{out} = Q$, WE CAN IMMEDIATLY SAY THAT $V_{out\,DC} = Q$ SO WHEN $Q = 1$ WE HAVE THE MAXIMUM DC AND SO THE MAXIMUM PHASE SHIFT. AFTER THE MAXIMUM PHASE SHIFT VALUE, CLEARLY THE CHARACTERISTIC STARTS OVER FROM 0, WE CAN SEE THAT THIS TYPE OF PD CAN HANDLE A FULL PERIOD OF 2π WITHOUT CHANGING THE POLARITY: IT COULD BE A GOOD OR NEGATIVE FACT ACCORDING TO THE TYPE OF PD WE WANT TO REALIZE. A PROBLEM OF THIS TYPE OF PD IS RELEATED TO THE FACT THAT S AND R CAN'T COMMUTE IN THE SAME INSTANT: IT CAUSES THE FORBIDDEN AREAS IN THE CHARACTERISTIC.

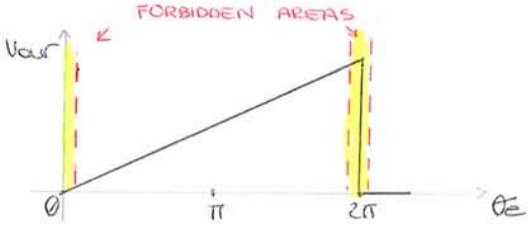

FIG C2.12 SR-Flip Flop characteristic

IN ORDER TO SOLVE THIS PROBLEM, WE CAN USE TWO TECHNIQUES:

- WE CAN USE FREQUENCY DIVIDERS THAT MANTAIN CONSTANT THE RELATION BETWEEN THE SIGNALS BUT CHANGE THEIR PERIOD AND PHASE SHIFT IN ORDER TO HAVE NO OVERLAPS
- WE CAN USE PD THAT CAN OPERATE DIRECTLY ON THESE SIGNALS, USING FINE STATE MACHINES THAT CAN PREDICT THE SIGNAL'S PROBLEMS AND, IF THEY'RE EDGE SENSITIVE, RESOLVE THEM (IE. MASTER-SLAVE FLIPFLOP).

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3) CHARGE PUMP PDS

WE INTRODUCED CHARGE PUMP CIRCUITS IN LESSON C1 AND ANALYZED THEIR USE AS FILTER OR AMPLIFIER. NOW WE WANT TO UNDERSTAND HOW THEY CAN WORK AS PDS. LET'S SEE WHAT HAPPENS FOR DIFFERENT COMBINATIONS OF THE INPUT SIGNALS AND, SO, OF A AND B:

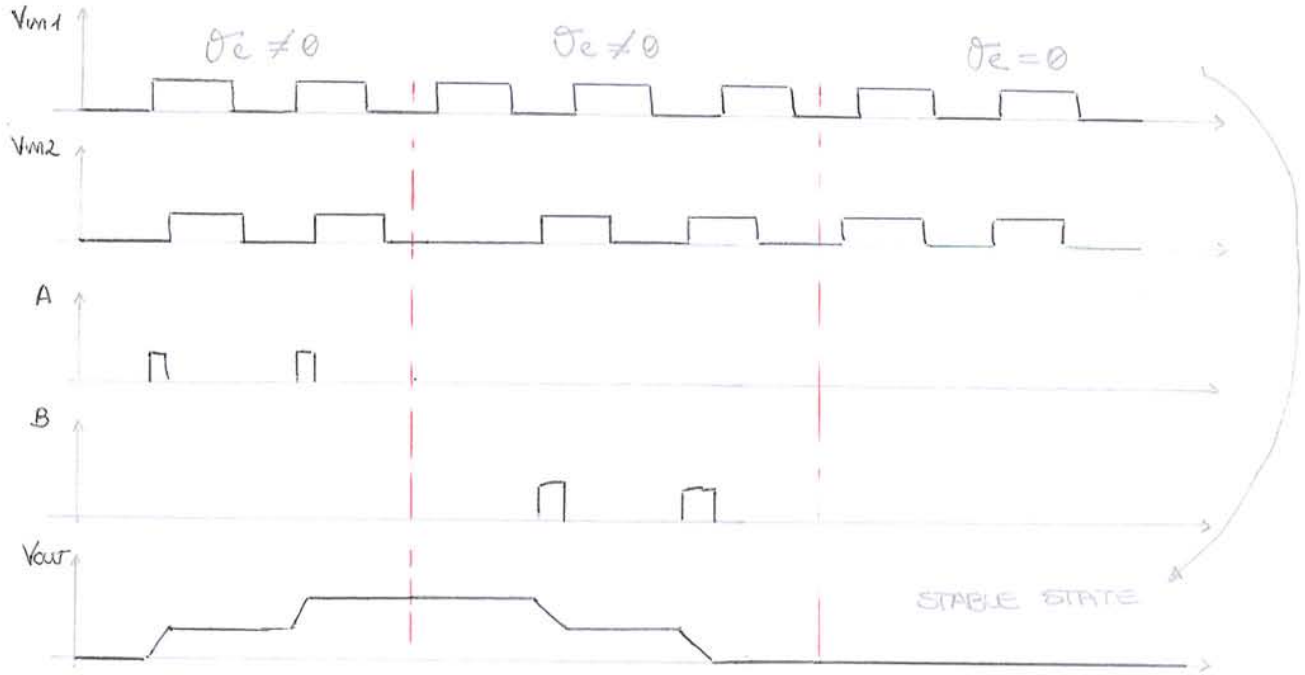

FIG C2.13 Charge Pump PDs behaviour

THE EQUIVALENT LOOP GAIN FOR ALL WITH CP IS AN ∞ LOOP GAIN. SO WE CAN SAY THAT WHEN THERE IS A PHASE SHIFT WE HAVE AN UNSTABLE STATE; THE ONLY STABLE STATE IS OBTAINED FOR $\theta_e = 0$.

IN THE END, WE CAN DO SOME COMPARISON BETWEEN ANALOG AND DIGITAL PDS. THE FIRST ONE REGARDS THE CHARACTERISTIC AND THE USABLE RANGE: IF WE USE XOR PDS IT'S THE SAME BUT IF WE USE SR LATCH IT'S DOUBLED. HOWEVER, WE'VE OTHER LIMITATIONS DUE TO THE USE OF SR LATCH PDS. THE DIGITAL PDS ALLOW A MORE REALISTIC ANALYSIS WHEN WE ASSUME A LINEAR PD, PLUS WE'VE A GREATER OUTPUT EXCURSION.

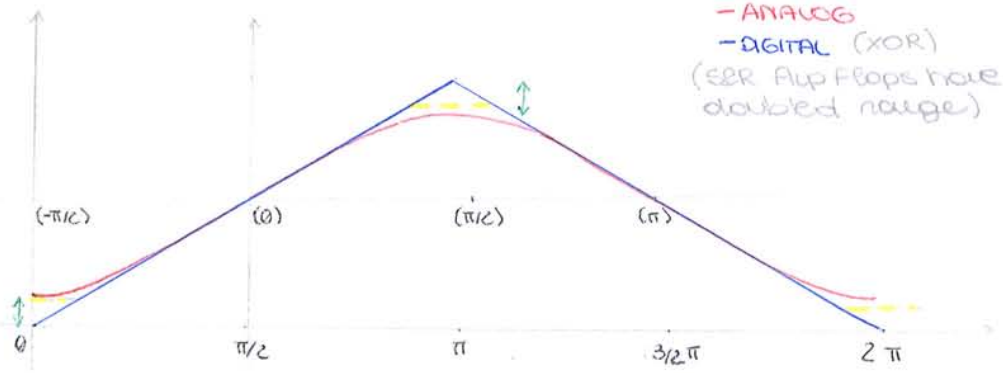

FIG C2.14 Analog vs. Digital (XOR) characteristic

NOW WE'RE GOING TO APPLY AN INPUT SIGNAL OF VARIABLE FREQUENCY; IMAGE TO INCREASE ω_{in} SLOWLY, STEP BY STEP.

- $\omega_{in} \ll \omega_{OR}$ → THE VD IS QUITE TOTALLY FILTERED BY THE FILTER, SO WE CAN'T MODIFY THE ω_{OUT}.
- ω_{in} ↑ → WE'RE MOVING "TO THE RIGHT" : VD IS NOT COMPLETELY FILTERED, V_C INCREASES ITS AMPLITUDE AND ω_{OUT} CHANGE IS HIGHER.
- ω_{in}: THERE'S AN INTERCEPTION BETWEEN THE VCO AND THE BUTTERFLY CHARACTERISTICS, WE'LE THAT V_C IS HIGH ENOUGH TO MODIFY ω_{OUT}, SO WE OBTAIN THE LOCK CONDITION.
- ω_{in} ↑ → NOW WE'RE DEALING WITH ONLY DC TERMS, BECAUSE WE'RE ONLY CORRECTING ω_{OUT} WITH LOW VALUES RESPECT TO ω_{in}.

THE LOCK CONDITION IS MANTEINED OVER THE SYMMETRIC FILTER RESPONSE!

- ω_{in} : THERE'S AN INTERCEPTION BETWEEN VCO CARACTERISTIC AND F(Ø) GAIN, WE'LE TO GIVE TO THE VCO A VOLTAGE HIGHER THAN THE ONE THAT FILTER CAN LET PASS THROUGH ITSELF BECAUSE OF THE DC GAIN.

THE LOCK CONDITION IS LOST; WE CAN OBTAIN IT ONLY GOING BACK UNTIL THE INTERCEPTION!

A SIMILAR BEHAVIOUR CAN BE OBSERVED IF WE DECREAS ω_{in}, STARTING FROM A VERY HIGH VALUE, AS SHOWN IN FIG C3.7

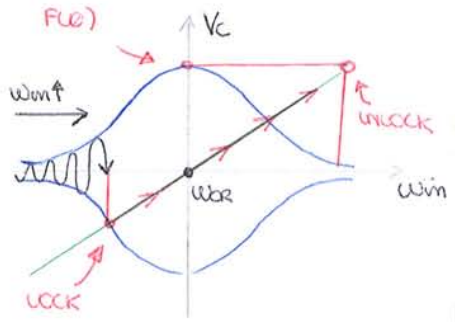

FIG C3.6 Behaviour of PLL for ω_{in} increasing (FORWARD)

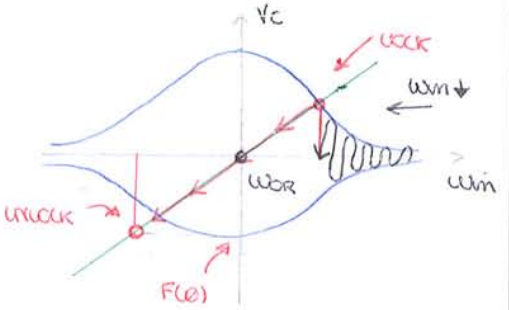

FIG C3.7 Behaviour of PLL for ω_{in} decreasing (BACKWARD)

SO, WE CAN DEFINE TWO FREQUENCY RANGES:

- **CAPTURE RANGE** : THE RANGE OF FREQUENCIES FROM LOCK TO UNLOCK CONDITION. IT'S THE SYMMETRIC RANGE OF VALUES WHERE WE CAN OBTAIN THE LOCK CONDITION WITHOUT HAVING IT BEFORE AND WHERE THE SYSTEM IS LOCK AND STAY LOCK.
- **LOCK-IN RANGE** : THE RANGE OF FREQUENCIES WHERE IF WE'VE LOCK WE CONTINUE TO HAVE LOCK BUT IF WE DIDN'T HAVE LOCK, WE CAN'T HAVE LOCK.

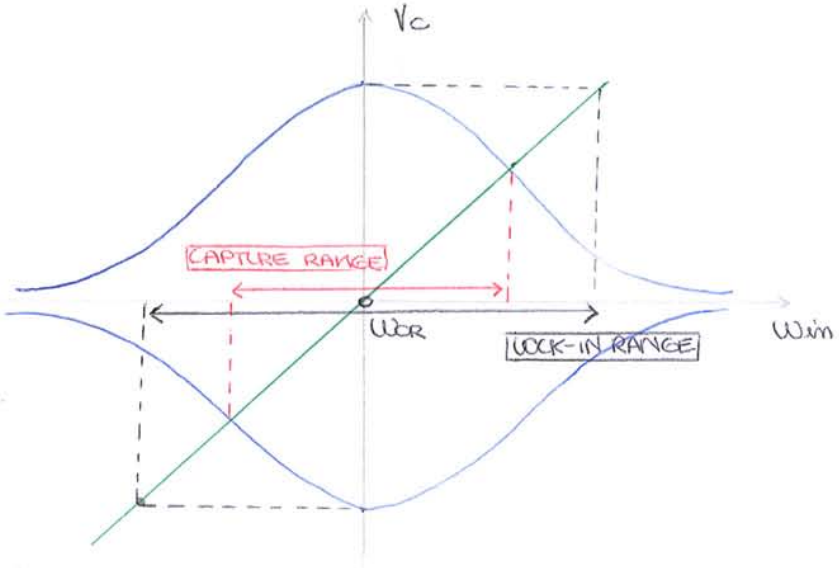

FIG C3.8 Lock-in and Capture ranges